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WHITE PAPER

MARVELL® ThunderX2® PMU Events (Abridged)

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INTRODUCTION

The Arm architecture defines several events as part of the Performance Monitor Unit (PMU) Extension. The Marvell ThunderX2 CN99XX processor implements the "required events" as documented in section D5.10.7 of the "Arm Architecture Reference Manual Armv8, for Armv8-A architecture profile". In addition, herein, we document those "IMPLEMENTATION DEFINED" events which Marvell deems most useful for analyzing performance.

More details for the registers and the mechanisms to access them are discussed in this document.

COUNTING ACROSS THREADS

The Armv8 Debug Architecture provides a control bit (MT) in the Event Type registers to enable counting across threads for a CPU core which supports multiple hardware threads. For a first thread to count events from a second thread, both threads must be allowed to count.

Event Number	Event Type	Event Mnemonic	Description
0x0000	A	SW_INCR	Instruction architecturally executed, condition code check pass, software increment.
0x0001	M	L1I_CACHE_REFILL	Level 1 instruction cache refill.
0x0002	M	L1I_TLB_REFILL	Level 1 instruction TLB refill.
0x0003	M	L1D_CACHE_REFILL	Level 1 data cache refill.
0x0004	M	L1D_CACHE	Level 1 data cache access.
0x0005	M	L1D_TLB_REFILL	Level 1 data TLB refill.
0x0006	A	LD_RETIRED	Instruction architecturally executed, condition code check pass, load.
0x0007	A	ST_RETIRED	Instruction architecturally executed, condition code check pass, store.
0x0008	A	INST_RETIRED	Instruction architecturally executed.
0x0009	A	EXC_TAKEN	Exception taken.
0x000A	A	EXC_RETURN	Instruction architecturally executed, condition code check pass, exception return.
0x000B	A	CID_WRITE RETIRED	Instruction architecturally executed, condition code check pass, write to CONTEXTIDR.
0x000D	A	BR_IMMED_RETIRED	Instruction architecturally executed, immediate branch.
0x000E	A	BR_RETURN_RETIRED	Instruction architecturally executed, condition code check pass, procedure return.
0x000F	A	UNALIGNED_LDST_RETIRED	Instruction architecturally executed, condition code check pass, unaligned load or store.
0x0010	M	BR_MIS_PRED	Mispredicted or not predicted branch speculatively executed.
0x0011	M	CPU_CYCLES	Cycle.
0x0012	M	BR_PRED	Predictable branch speculatively executed.
0x0013	M	MEM_ACCESS	Data memory access.
0x0014	M	L1I_CACHE	Level 1 instruction cache access.

Event Number	Event Type	Event Mnemonic	Description
0x0015	M	L1D_CACHE_WB	Level 1 data cache write-back.
0x0016	M	L2D_CACHE	Level 2 data/unified cache access.
0x0017	M	L2D_CACHE_REFILL	Level 2 data/unified cache refill.
0x0018	M	L2D_CACHE_WB	Level 2 data/unified cache write back.
0x0019	M	BUS_ACCESS	Bus access.
0x001B	M	INST_SPEC	Operation speculatively executed.
0x001C	A	TTBR_WRITE_RETIRED	Instruction architecturally executed, condition code check pass, write to TTBR.
0x001E	A	CHAIN	For odd-numbered counters, increments the count by one for each overflow of the preceding even numbered counter.
0x001F	M	L1D_CACHE_ALLOCATE	Level 1 data cache allocation without refill.
0x0020	M	L2D_CACHE_ALLOCATE	Level 2 data/unified cache allocation without refill.
0x0021	A	BR_RETIRED	Counts all branches on the architecturally executed path that would incur cost if mispredicted.
0x0022	A	BR_MIS_PRED_RETIRED	Instruction executed, mispredicted branch. All instructions counted by BR RETIRED that were not correctly predicted.
0x0023	M	STALL_FRONTEND	Cycle on which no operation issued because there are no operations to issue.
0x0024	M	STALL_BACKEND	Cycle on which no operation issued due to back-end resources being unavailable.
0x0025	M	L1D_TLB	Level 1 data TLB access.
0x0026	M	L1I_TLB	Level 1 instruction TLB access.
0x002D	M	L2D_TLB_REFILL	Attributable memory-read/write operation that causes a TLB refill of at least the Level 2 data or unified TLB
0x002E	M	L2I_TLB_REFILL	Attributable instruction memory accesses that cause a TLB refill of at least the Level 2 instruction or unified TLB.
0x002F	M	L2D_TLB	Attributable memory read/write operation that causes a TLB access to at least the Level 2 data or unified TLB.
0x0030	M	L2I_TLB	Attributable memory read/write operation that causes a TLB access to at least the Level 2 instruction or unified TLB. MMU.
0x0040	M	L1D_CACHE_RD	Level 1 data cache access, read.
0x0041	M	L1D_CACHE_WR	Level 1 data cache access, write.
0x0042	M	L1D_CACHE_REFILL_RD	Level 1 data cache refill, read.
0x0042	M	L1D_CACHE_REFILL_RD	Level 1 data cache refill, read.

Event Number	Event Type	Event Mnemonic	Description
0x0043	M	L1D_CACHE_REFILL_WR	Level 1 data cache refill, write.
0x0044	M	L1D_CACHE_REFILL_INNER	Level 1 data.
0x0045	M	L1D_CACHE_REFILL_OUTER	Level 1 data cache refill, outer.
0x0046	M	L1D_CACHE_WB_VICTIM	Level 1 data cache write-back, victim (threadless).
0x0047	M	L1D_CACHE_WB_CLEAN	Level 1 data cache write-back, cleaning and coherency (thread-less).
0x0048	M	L1D_CACHE_INVAL	Level 1 data cache invalidate (threadless).
0x004C	M	L1D_TLB_REFILL_RD	Level 1 data TLB refill, read.
0x004D	M	L1D_TLB_REFILL_WR	Level 1 data TLB refill, write.
0x004E	M	L1D_TLB_RD	Level 1 data TLB access, read.
0x004F	M	L1D_TLB_WR	Level 1 data TLB access, write.
0x0050	M	L2D_CACHE_RD	Level 2 data cache access, read.
0x0051	M	L2D_CACHE_WR	Level 2 data cache access, write.
0x0052	M	L2D_CACHE_REFILL_RD	Level 2 data cache refill, read.
0x0053	M	L2D_CACHE_REFILL_WR	Level 2 data cache refill, write.
0x0056	M	L2D_CACHE_WB_VICTIM	Level 2 data cache write-back, victim.
0x0057	M	L2D_CACHE_WB_CLEAN	Level 2 data cache write-back, cleaning and coherency.
0x0058	M	L2D_CACHE_INVAL	Level 2 data cache invalidate.
0x005C	M	L2D_TLB_REFILL_RD	Level 2 data/unified TLB refill, read.
0x005D	M	L2D_TLB_REFILL_WR	Level 2 data/unified TLB refill, write.
0x005E	M	L2D_TLB_RD	Level 2 data/unified TLB access, read.
0x005F	M	L2D_TLB_WR	Level 2 data/unified TLB access, read.
0x0060	M	BUS_ACCESS RD	Bus access, read.
0x0061	M	BUS_ACCESS_WR	Bus access, write.
0x0062	M	BUS_ACCESS_SHARED	Bus access, Normal, Cacheable, Shareable.
0x0063	M	BUS_ACCESS_NOT_SHARED	Bus access, not Normal, Cacheable, Shareable.
0x0064	M	BUS_ACCESS_NORMAL	Bus access, normal.
0x0065	M	BUS_ACCESS_PERIPH	Bus access, peripheral.
0x0066	M	MEM_ACCESS_RD	Data memory access, read.
0x0067	M	MEM_ACCESS_WR	Data memory access, write.

Event Number	Event Type	Event Mnemonic	Description
0x0068	M	UNALIGNED_LD_SPEC	Unaligned access, read.
0x0069	M	UNALIGNED_ST_SPEC	Unaligned access, write (threadless).
0x006A	M	UNALIGNED_LDST_SPEC	Unaligned access (threadless).
0x006C	M	LDREX_SPEC	Exclusive operation speculatively executed, LDREX or LDX.
0x006D	M	STREX_PASS_SPEC	Exclusive operation speculatively executed, STREX or STX pass.
0x006E	M	STREX_FAIL_SPEC	Exclusive operation speculatively executed, STREX or STX pass.
0x006F	M	STREX_SPEC	Exclusive operation speculatively executed, STREX or STX.
0x0070	M	LD_SPEC	Operation speculatively executed, load.
0x0071	M	ST_SPEC	Operation speculatively executed, store.
0x0072	M	LDST_SPEC	Operation speculatively executed, load or store.
0x0073	M	DP_SPEC	Operation speculatively executed, integer data processing.
0x0074	M	ASE_SPEC	Operation speculatively executed, Advanced SIMD instruction.
0x0075	M	VFP_SPEC	Operation speculatively executed, floating-point instruction.
0x0077	M	CRYPTO_SPEC	Operation speculatively executed, Cryptographic instruction.
0x0078	M	BR_IMMED_SPEC	Branch speculatively executed, immediate branch.
0x0079	M	BR_RETURN_SPEC	Branch speculatively executed, procedure return.
0x007A	M	BR_INDIRECT_SPEC	Branch speculatively executed, indirect branch.
0x007C	M	ISB_SPEC	Barrier speculatively executed, ISB.
0x007D	M	DSB_SPEC	Barrier speculatively executed, DSB.
0x007E	M	DMB_SPEC	Barrier speculatively executed, DMB.
0x0081	A	EXC_UNDEF	Exception taken, Other synchronous.
0x0082	A	EXC_SVC	Exception taken, Supervisor Call.
0x0083	A	EXC_PABORT	Exception taken, Instruction Abort.
0x0084	A	EXC_DABORT	Exception taken, Data Abort and SError.
0x0086	A	EXC_IRQ	Exception taken, IRQ.
0x0087	A	EXC_FIQ	Exception taken, FIQ.
0x0088	A	EXC_SMC	Exception taken, Secure Monitor Call.

Event Number	Event Type	Event Mnemonic	Description
0x008A	A	EXC_HVC	Exception taken, Hypervisor Call.
0x008B	A	EXC_TRAP_PABORT	Exception taken, Instruction Abort not taken locally.
0x008C	A	EXC_TRAP_DABORT	Exception taken, Data Abort or SError not taken locally.
0x008D	A	EXC_TRAP_OTHER	Exception taken, Other traps not taken locally.
0x008E	A	EXC_TRAP_IRQ	Exception taken, IRQ not taken locally.
0x008F	A	EXC_TRAP_FIQ	Exception taken, FIQ not taken locally.
0x0090	M	RC_LD_SPEC	Release consistency operation speculatively executed, Load Acquire.
0x0091	M	RC_ST_SPEC	Release consistency operation speculatively executed, Store Release.
0x00C1	M	L1D_LHS_VANOTP	A Load hit store retry. VA match against an older entry in the SRQ but the PA mismatches.
0x00C2	M	L1D_LHS_OVRLAP	Load hit store retry. VA match against an older entry in the SRQ but the required load bytes are not all contained.
0x00C3	M	L1D_LHS_VANOSD	Load hit store retry. VA match against an older entry in the SRQ but the associated store data has not been issued yet.
0x00C4	M	L1D_LHS_FWD	Load hit store forwarding. Load completes with data successfully forwarded from the SRQ.
0x00C6	M	L1D_BNKCFL	Bank Conflict load retry. A load that hits in the L1 retries due a bank read conflict with another higher priority port of the L1.
0x00C7	M	L1D_LSMQ_FULL	LSMQ full retry. A load misses the L1 but retries due to the LSMQ being full. Upon retry, sleep in the SCH until a fill return.
0x00C8	M	L1D_LSMQ_HIT	LSMQ hit retry. A load misses the L1 but retries due to hitting an LSMQ that already has 2 loads al-located to it.
0x00C9	M	L1D_EXPB_MISS	An external probe missed the L1.
0x00CA	M	L1D_L2EV_MISS	An L2 Evict operation missed the L1.
0x00CB	M	L1D_EXPB_HITM	An external probe hit a modified line in the L1. (threadless).
0x00CC	M	L1D_L2EV_HITM	An L2 Evict operation hit a modified line in the L1. (threadless).
0x00CD	M	L1D_EXPB_HIT	An external probe hit in the L1. (threadless).
0x00CE	M	L1D_L2EV_HIT	An L2 Evict operation hit in the L1. (threadless).
0x00CF	M	L1D_EXPB_RETRY	An external probe hit was retried by the LSU. (threadless).
0x00D0	M	L1D_L2EV_RETRY	An L2 Evict operation was retried by the LSU. (threadless).

Event Number	Event Type	Event Mnemonic	Description
0x00D1	M	L1D_ST_RMW	A read modify write store was drained and updated the L1. A RmW store is any store that up-dates 1, 2, or 3 bytes of a bank.
0x00D2	M	L1D_LSMQ00_LDREQ	A load has allocated LSMQ entry 0 and made a request to the SCU.
0x00D3	M	L1D_LSMQ00_LDVLD	LSMQ entry 0 was initiated by a load and is valid this cycle. (threadless).
0x00D4	M	L1D_LSMQ15_STREQ	A store has allocated LSMQ entry 15 and made a request to the SCU.
0x00D5	M	L1D_LSMQ15_STVLD	LSMQ entry 15 was initiated by a store and is valid this cycle. (threadless).
0x00D6	M	L1D_PB_FLUSH	LRQ ordering flush.
0x00E0	A	BR_COND_MIS_PRED_RETIRED	Conditional branch instruction executed, but mis-predicted.
0x00E1	A	BR_IND_MIS_PRED_RETIRED	Indirect branch instruction executed, but mis-predicted.
0x00E2	A	BR_RETURN_MIS_PREDRETIRED	Return branch instruction executed, but mis-predicted.
0x00E8	M	OP_RETIRED	Uops executed.
0x00E9	M	LD_OP_RETIRED	Load uops executed.
0x00EA	M	ST_OP_RETIRED	Store uops executed.
0x00EB	M	FUSED_OP_RETIRED	Fused uops executed.
0x00F8	A	IRQ_MASK	Cumulative duration of a PSTATE.I interrupt mask set to 1.
0x00F9	A	FIQ_MASK	Cumulative duration of a PSTATE.F interrupt mask set to 1.
0x00FA	A	SERROR_MASK	Cumulative duration of a PSTATE.A interrupt mask set to 1.
0x0108	M	WFIWFE_SLEEP	Count every cycle in which the CPU is asleep due to having entered a low power mode on executing a WFI or WFE instruction.
0x0127	M	L2TLB_4K_PAGE_MISS	L2 TLB lookup miss using 4K page size.
0x0128	M	L2TLB_64K_PAGE_MISS	L2 TLB lookup miss using 64K page size.
0x0129	M	L2TLB_2M_PAGE_MISS	L2 TLB lookup miss using 2M page size.
0x012A	M	L2TLB_512M_PAGE_MISS	L2 TLB lookup miss using 512M page size.
0x0150	M	ISB_EMPTY	Number of cycles during which micro-op skid-buffer in empty.
0x0151	M	ISB_FULL	Num of cycles uop skid-buffer is back-pressuring decode. (5 or more entries are occupied).
0x0152	M	STALL_NOTSELECTED	Number of cycles during which thread was available for dispatch but was not selected.
0x0153	M	ROB_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch due to ROB full.

Event Number	Event Type	Event Mnemonic	Description
0x0154	M	ISSQ_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch because the instruction issue queue is full.
0x0155	M	GPR_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch because GPR renamer pool is empty.
0x0156	M	FPR_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch because the FPR renamer pool is empty.
0x0158	M	LRQ_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch due to LRQ full.
0x0159	M	SRQ_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch due to SRQ full.
0x015B	M	BSR_RECYCLE	Number of cycles in which one or more valid micro-ops did not dis-patch because the branch check-point buffer is full.
0x0164	M	UOPSFUSED	Number of fused micro-ops dispatched.
0x020B	M	L2D_TLBI_INT	Internal mmu tlbi cacheops.
0x020C	M	L2D_TLBI_EXT	External mmu tlbi cacheops.
0x0218	M	L2D_HWPF_DMD_HIT	Scu ld/st requests that hit cache or msq for lines brought in by the hardware prefetcher.
0x0219	M	L2D_HWPF_REQ_VAL	Scu hwpf requests into the pipeline.
0x021A	M	L2D_HWPF_REQ_LD	Scu hwpf ld requests into the pipeline.
0x021B	M	L2D_HWPF_REQ_MISS	Scu hwpf requests that miss.
0x021C	M	L2D_HWPF_NEXT_LINE	Scu hwpf next line requests generated.

UNCORE EVENTS - LAST LEVEL CACHE

Event Number	Event Type	Event Mnemonic	Description
0xD	M	L3_EVENT_READ_REQ	Number of Read requests received by the L3 Cache. This includes Read as well as Read Exclusives.
0xE	M	L3_EVENT_WRITEBACK_REQ	Number of Write Backs received by the L3 Cache. These are basically the L2 Evicts and writes from the PCIe Write Cache.
0x13	M	L3_EVENT_EVICT_REQ	Number of Evicts that the L3 cache generated.
0x17	M	L3_EVENT_READ_HIT	Number of Read requests received by the L3 cache that were hit in the L3 (Data provided form the L3).

UNCORE EVENTS - DDR CONTROLLER

Event Number	Event Type	Event Mnemonic	Description
0x1	M	DMC_EVENT_COUNT_CYCLES	Count cycles (Clocks at the DMC clock rate).
0xB	M	DMC_EVENT_WRITE_TXNS	Number of 64 Bytes write transactions received by the DMC(s)..
0xD	M	DMC_EVENT_DATA_TRANSFERS	Number of 64 Bytes data transferred to or from DRAM.
0xF	M	DMC_EVENT_READ_TXNS	Number of 64 Bytes Read transactions received by the DMC(s)

UNCORE EVENTS - CROSS SOCKET INTERCONNECT

Event Number	Event Type	Event Mnemonic	Description
0x3D	M	CCPI2_EVENT_REQ_PKT_SENT	Number of Requests packets that are sent form this node. A Request packet can contain one or two requests of any type. Some examples of requests types are, Reads, Read Exclusive, Writes and Evicts.
0x65	M	CCPI2_EVENT_SNOOP_PKT_SENT	Number of Snoops (coherency) packets that are sent from this node. A snoop packet can contain one or two snoops.
0x105	M	CCPI2_EVENT_DATA_PKT_SENT	Number of Data packets that are sent from this node. Data packet can be any size, but in general they are 64 bytes.
0x12D	M	CCPI2_EVENT_GIC_PKT_SENT	Number of Gic (interrupt related) packets that are sent from this node.

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