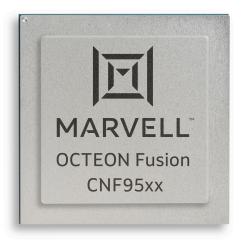


## OCTEON Fusion CNF95xx Press Briefing Presentation CNF95xx Product Introduction

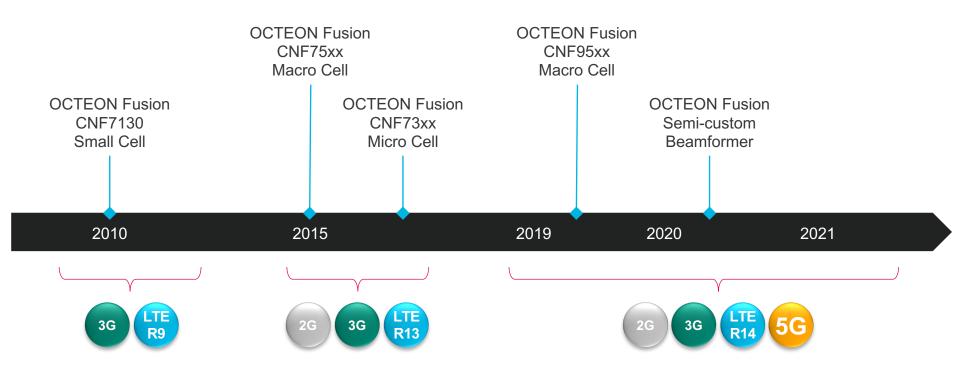
# Announcing Next Generation Family of OCTEON Fusion

- Industry-leading merchant silicon 5G macro cell baseband processor family
- Supports traditional all-in-one macro and disaggregated Distributed Unit (DU) base station architectures
- Delivers the performance of an ASIC with the flexibility of a processor
- May be tailored via differentiated IP integration on a per customer basis



CNF95xx is in volume production with a Tier 1 OEM

### A Long History of Compute Innovation



### **OCTEON Fusion CNF95xx Architecture**

\*Boot/Flash, eMMC, SPI, GPIO, UART, 12C

#### **PHY Subsystem**

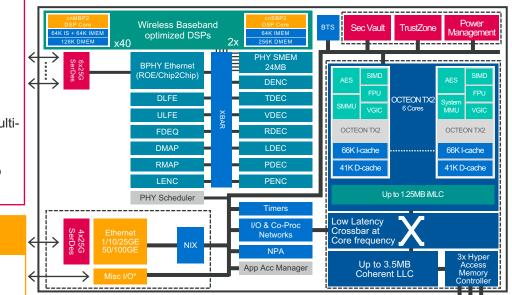
Software defined PHY subsysatem
Multi-core DSPs
4G/5G Specific HW accelerator blocks
Dedicated large internal SMEM
High-speed non-blocking multiported Interconnect Fabric
PHY Ethernet for radio and very low-latency chip-to-chip

#### SoC Interfaces

• 25G SerDes support

interface

- 100G/50G/25G/10G/1GbE support
- Application acceleration manager for core workload distribution
- Packet IO acceleration support



#### OCTEON TX2 CPU Cores

- Arm v8.2 Architecture, Up to 2.6 GHz
- Quad Issue, Out-of-order Pipeline
- 128b SIMD and floating-point support
- Full ARM virtualization spec supporteda

### Cache, Interconnect

Coherent MLC and LLC

2x 72b DDR4-2666

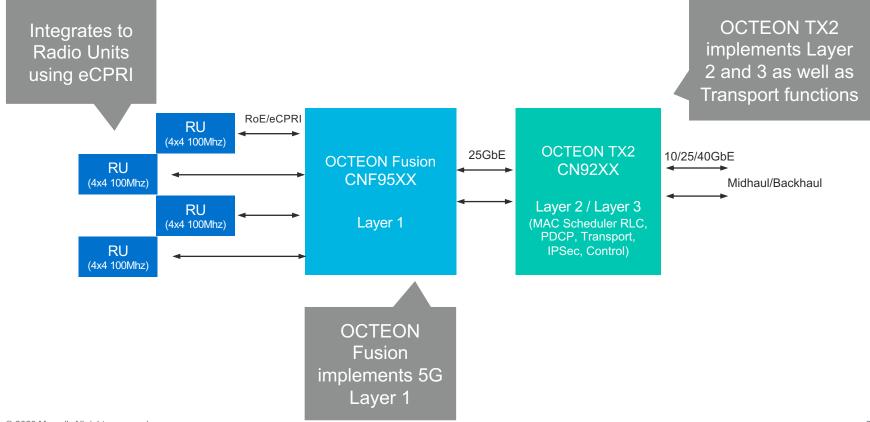
- Low-latency interconnect at core speed
- Up-to 2x DDR4-2666 MHz

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### **Multiple Business Model Options**

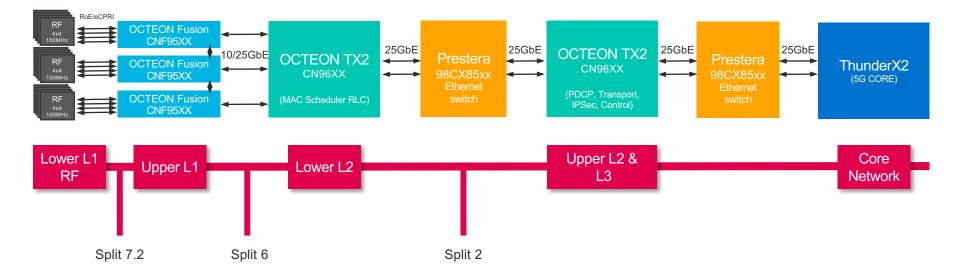


### 5G Macro Cell All-in-One Example



### 5G O-RAN Architecture Design Example

Marvell complete Portfolio enables 5G system architectures, such as the one proposed by the ORAN Alliance, to scale deployments and achieve the best OPEX and CAPEX in the industry



### **OCTEON Fusion – Key Takeaways**

- Industry-leading merchant silicon 5G macro cell baseband processor family
- Supports traditional all-in-one macro and disaggregated Distributed Unit (DU) base station architectures
- Delivers the performance of an ASIC with the flexibility of a processor
- Currently in Volume production with a Tier1





Essential technology, done right<sup>™</sup>