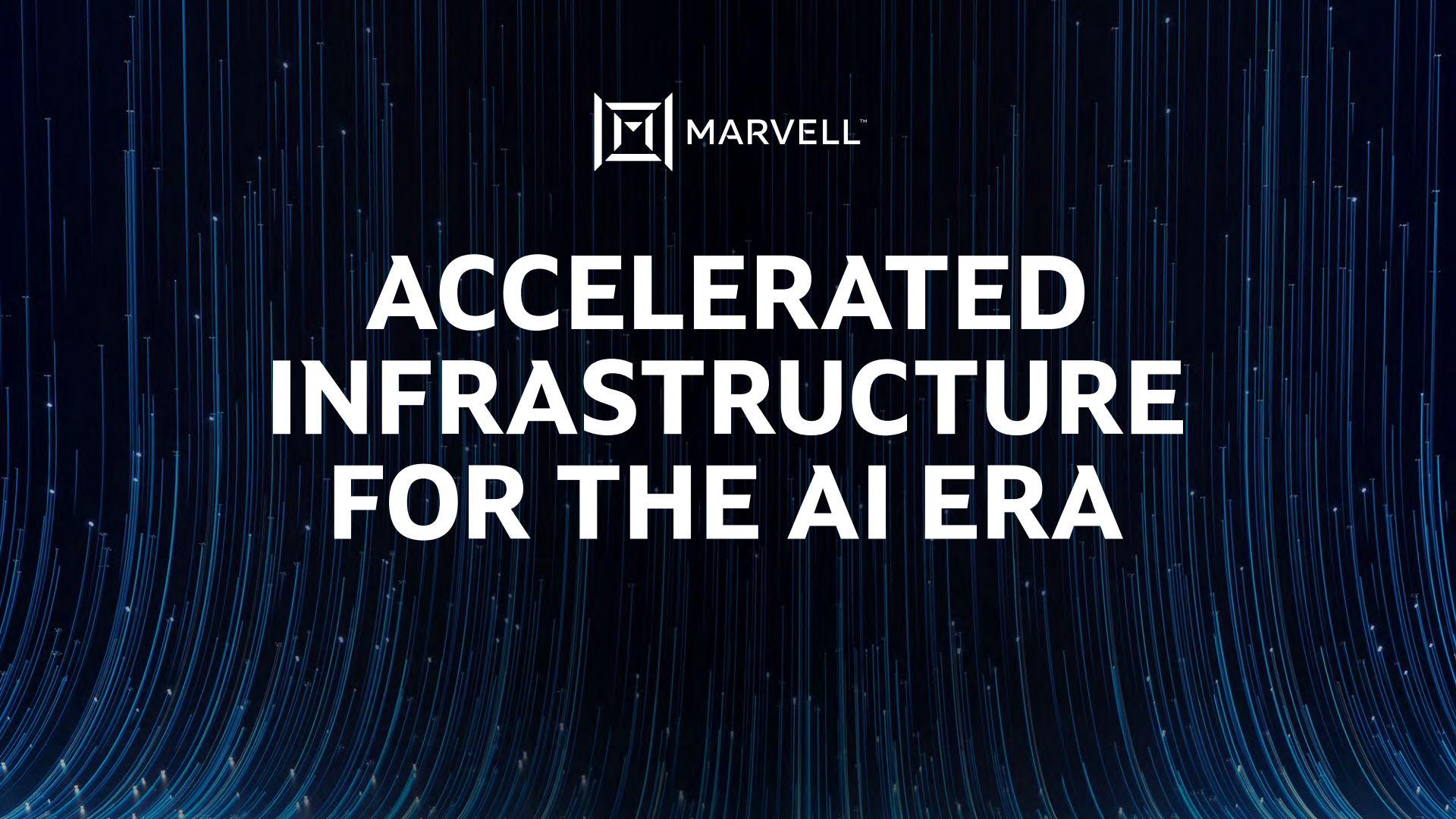

MARVELL
ACCELERATED
INFRASTRUCTURE
FOR THE AI ERA

Ashish Saran

Senior Vice President, Investor Relations

Agenda

Matt Murphy
Chairman and Chief Executive Officer

Loi Nguyen
EVP and GM, Cloud Optics

Achyut Shah
SVP and GM, Connectivity

Nick Kucharewski
SVP and GM, Network Switching

Raghib Hussain
President, Products and Technology

Q&A

Forward-looking statements

Except for statements of historical fact, this presentation contains forward-looking statements (within the meaning of the federal securities laws) including, but not limited to, statements related to market trends and to the company's business and operations, business opportunities, growth strategy and expectations, and financial targets and plans, that involve risks and uncertainties. Words such as "anticipates," "expects," "intends," "plans," "projects," "believes," "seeks," "estimates," "can," "may," "will," "would" and similar expressions identify such forward-looking statements. These statements are not guarantees of results and should not be considered as an indication of future activity or future performance. Actual events or results may differ materially from those described in this presentation due to a number of risks and uncertainties.

For factors that could cause Marvell's results to vary from expectations, please see the risk factors identified in Marvell's Annual Report on Form 10-K for the fiscal year ended February 3, 2024, as filed with the SEC on March 13, 2024, and other factors detailed from time to time in Marvell's filings with the SEC. The forward-looking statements in this presentation speak only as of the date of this presentation and Marvell undertakes no obligation to revise or update publicly any forward-looking statements.

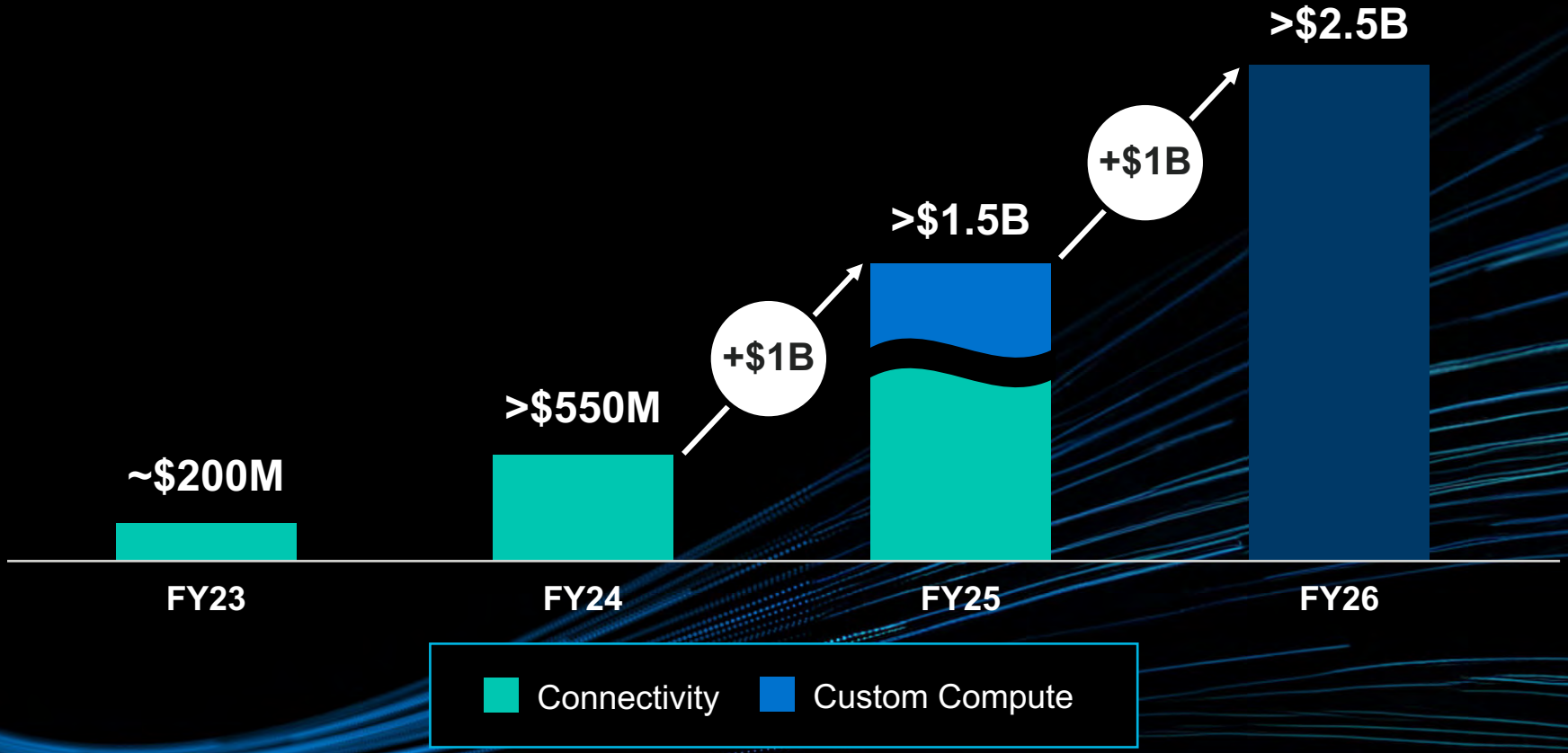
Non-GAAP financial measures

- During this presentation, we may refer to certain financial measures on a U.S. non-GAAP basis.
- We believe that the presentation of non-GAAP financial measures provides important supplemental information to management and investors regarding financial and business trends relating to our financial condition and results of operations.
- While we use non-GAAP financial measures as a tool to enhance our understanding of certain aspects of our financial performance, we do not consider these measures to be a substitute for, or superior to, the information provided by GAAP financial measures.
- A reconciliation in accordance with SEC Regulation G for non-GAAP financial measures is available in the Investor Relations section of our website at https://www.marvell.com.

Matt Murphy

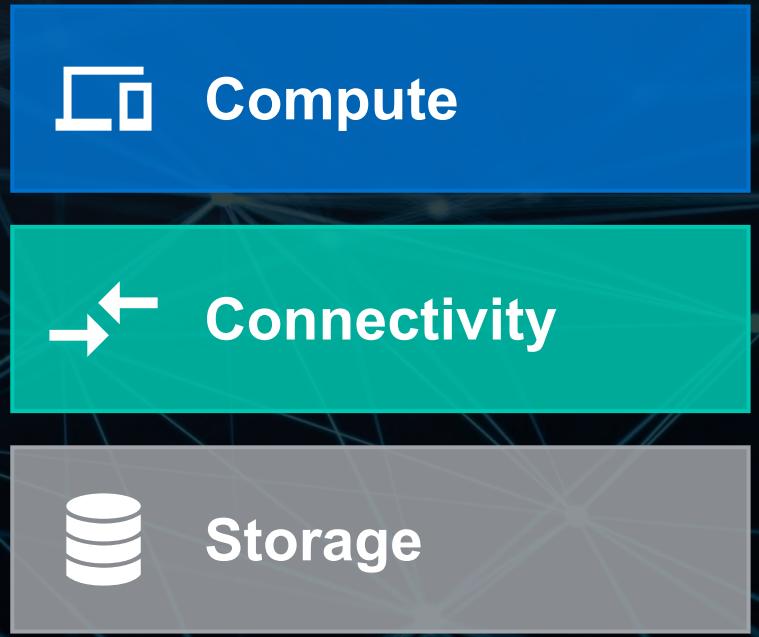
Chairman and Chief Executive Officer

Accelerating AI revenue for Marvell

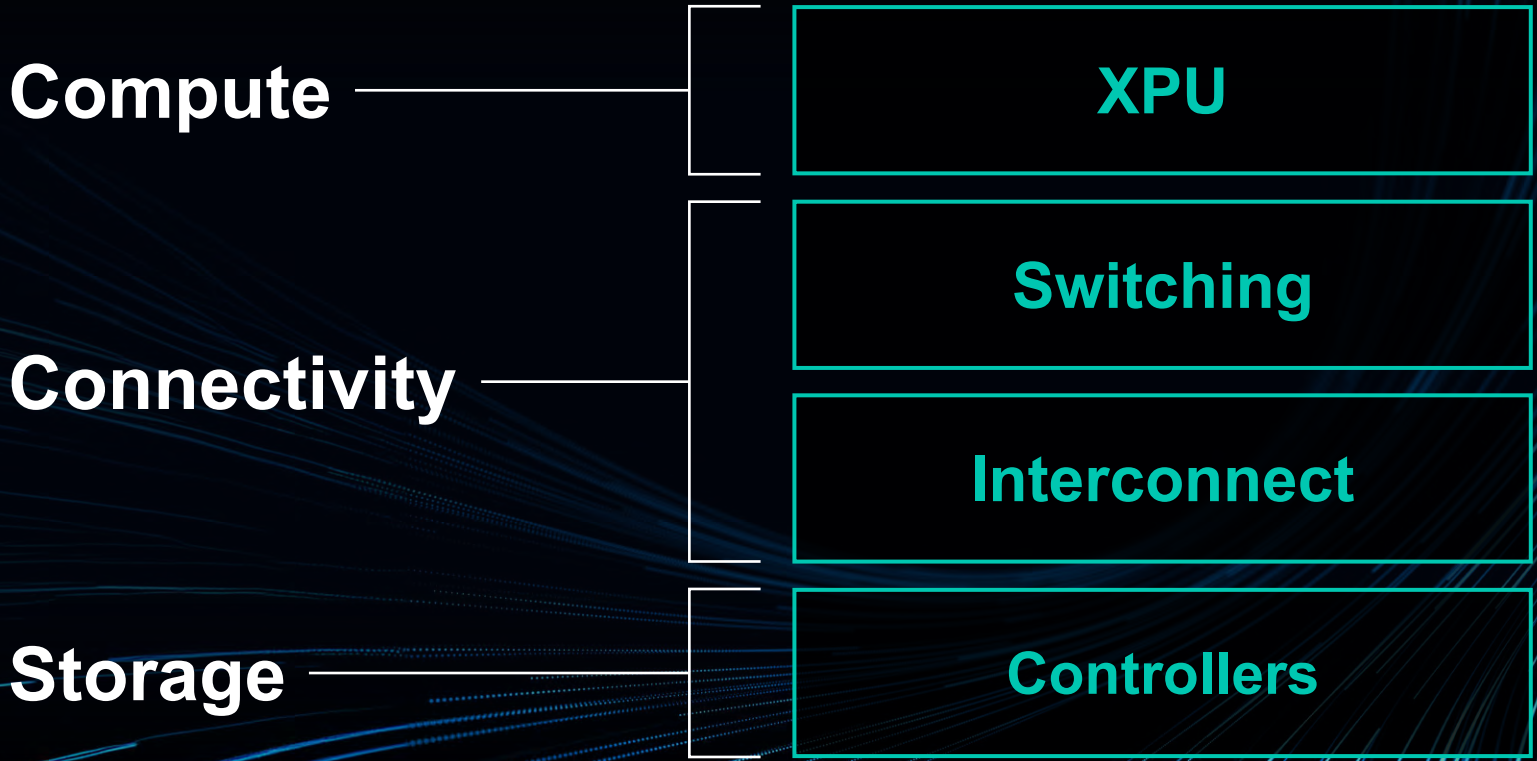


AI is the ultimate data infrastructure application

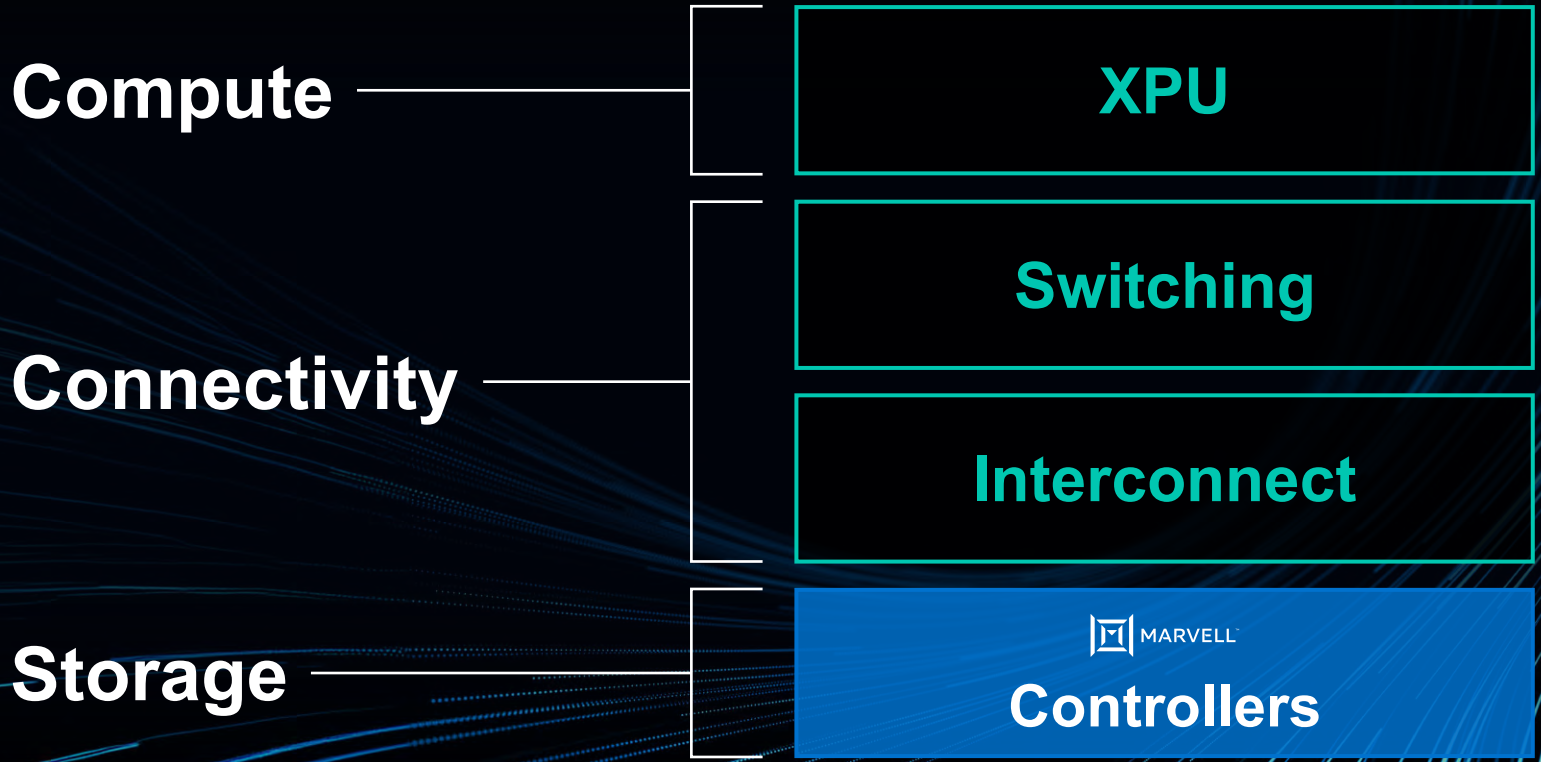
We develop and deliver semiconductor solutions that **move**, **store**, **process** and **secure** the world's **data** faster and more reliably than anyone else.



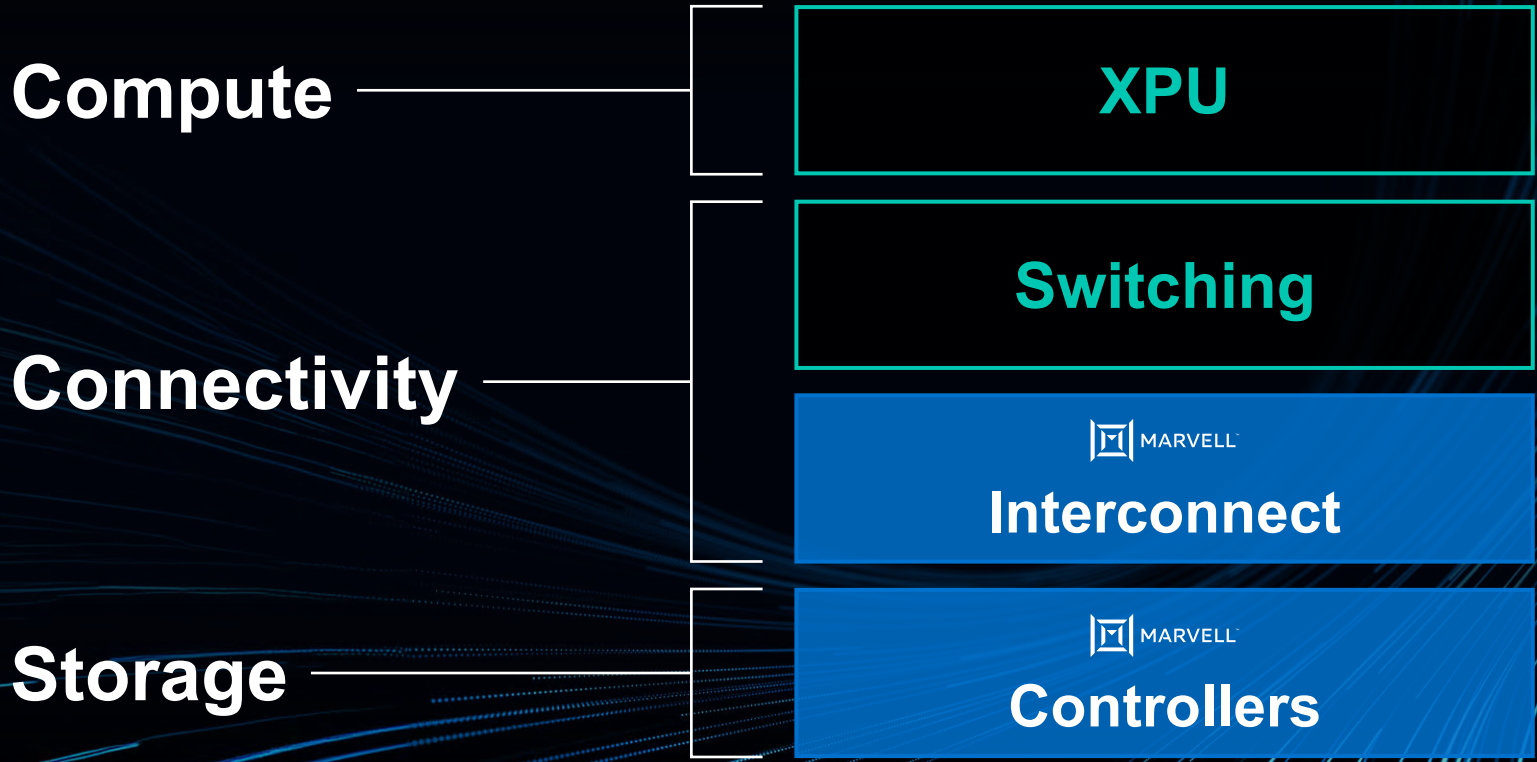
What is accelerated infrastructure?



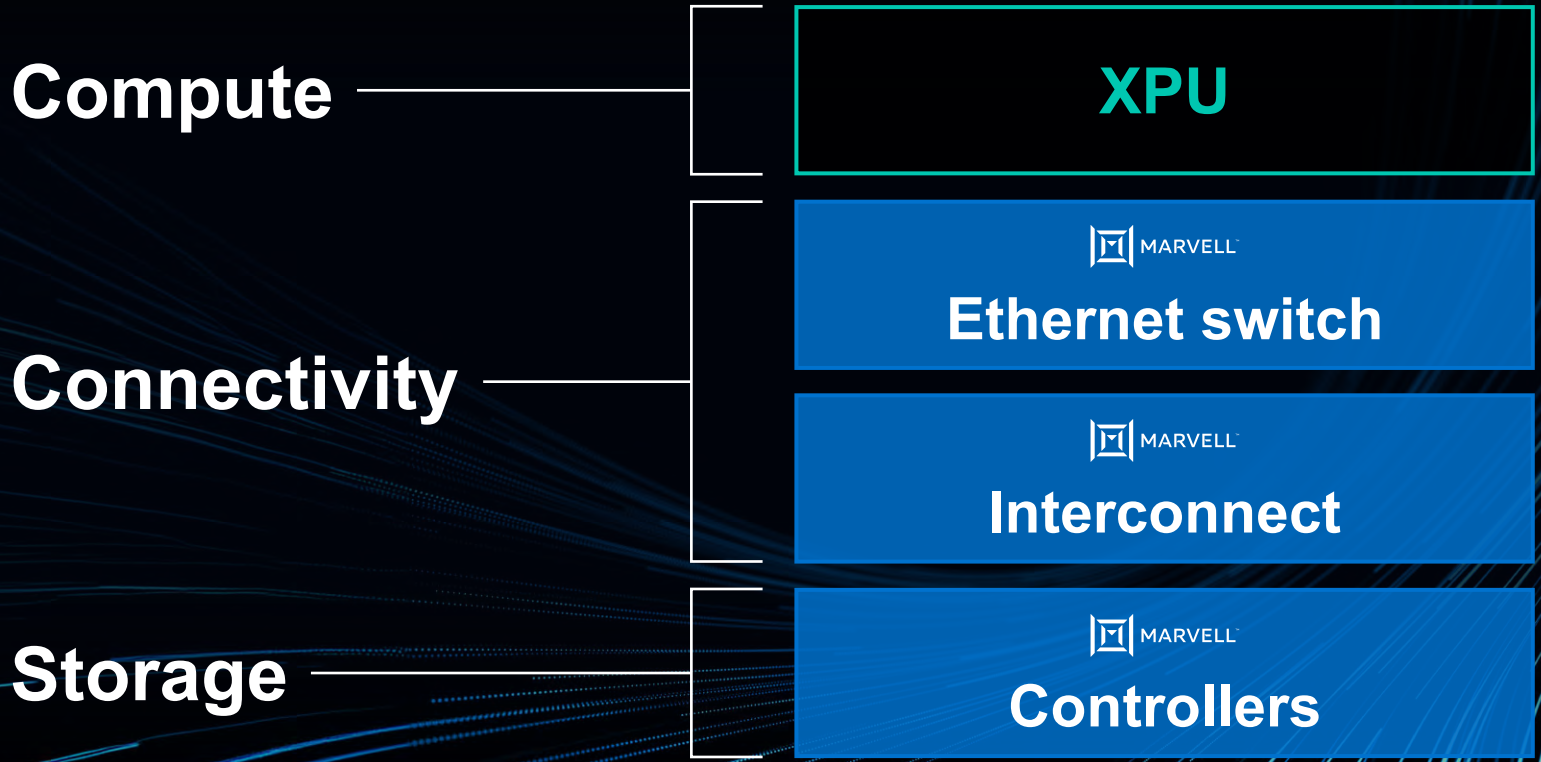
Marvell accelerated infrastructure



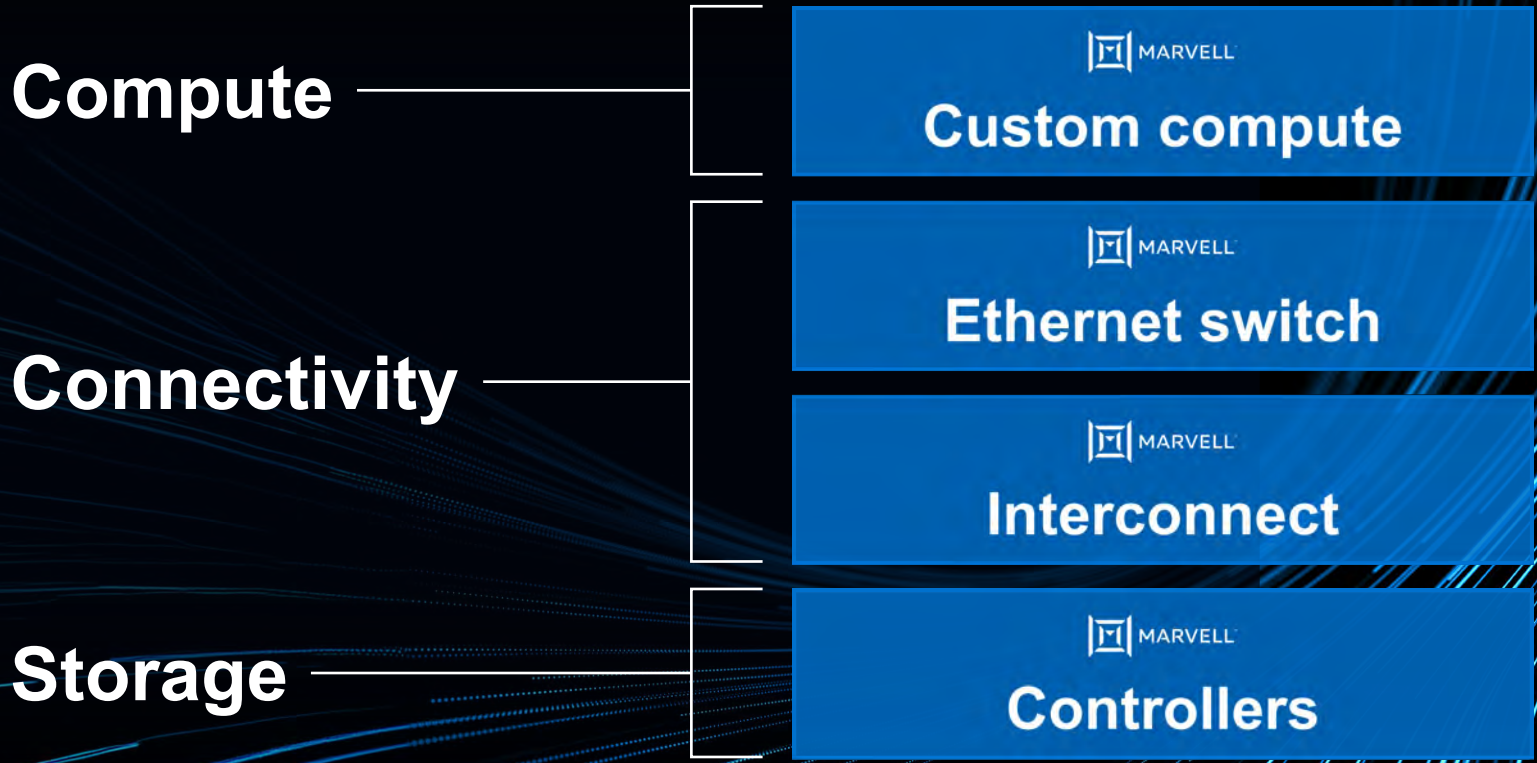
Marvell accelerated infrastructure



Marvell accelerated infrastructure



Marvell accelerated infrastructure

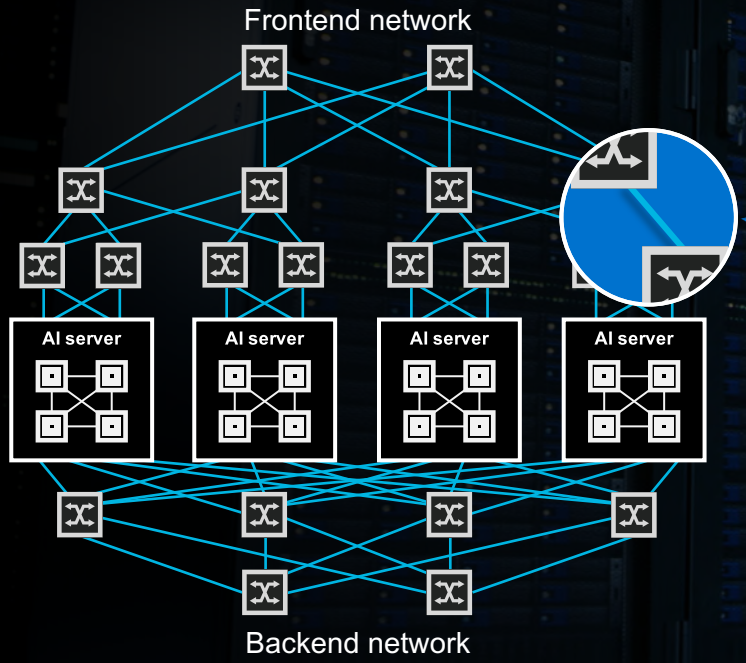


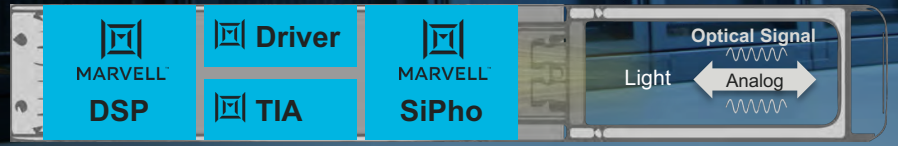
Interconnect in accelerated infrastructure

Custom compute

Ethernet switch

Interconnect



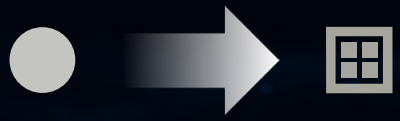


Connectivity foundational to accelerated computing

Custom compute
Ethernet switch
Interconnect

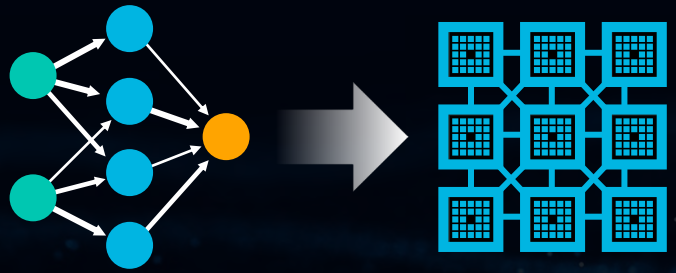
General purpose

One workload,
one processor



Accelerated

One workload,
many connected processors



Simple math of accelerated connectivity

Custom compute
Ethernet switch
Interconnect

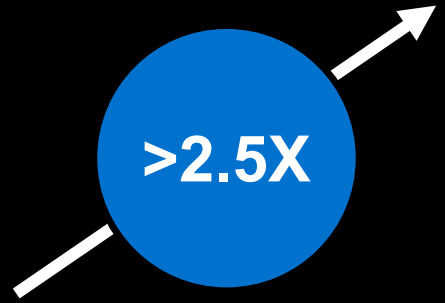
Number of ports | Port speed | Network hypergrowth

Massive TAM expansion

Investing to gain share in Ethernet switching for AI

Custom compute
Ethernet switch
Interconnect

Data center switching investment



At Innovium close

FY25

12.8 T

51.2 T

AI disruption creating new entry points

Partnering with customers for custom compute

Custom compute
Ethernet switch
Interconnect

2018 Investor Day

Emerging compute architectures for the Data Center

SECURITY AND NETWORK OFFLOAD

ARM SERVERS FOR CLOUD APPLICATIONS

ARTIFICIAL INTELLIGENCE

MARVELL® INVESTOR DAY 2018 78

2021 Investor Day

Cloud-optimized silicon

MARVELL INVESTOR DAY 2021 8

Multiple custom compute opportunities

Custom compute
Ethernet switch
Interconnect

Accelerated compute for AI

XPU

CPU

Custom compute

Security

NIC / DPU

Arm compute

Storage

Video

CXL

Simple math of custom compute

Custom compute
Ethernet switch
Interconnect

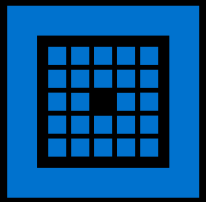
Massive TAM expansion

Expanding our AI customer base

Custom compute
Ethernet switch
Interconnect

NEW!

Customer A



AI training accelerator

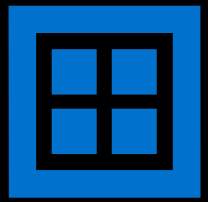
Ramping now

AI inference accelerator

CY2025 ramp

NEW!

Customer B



Arm CPU

Ramping now

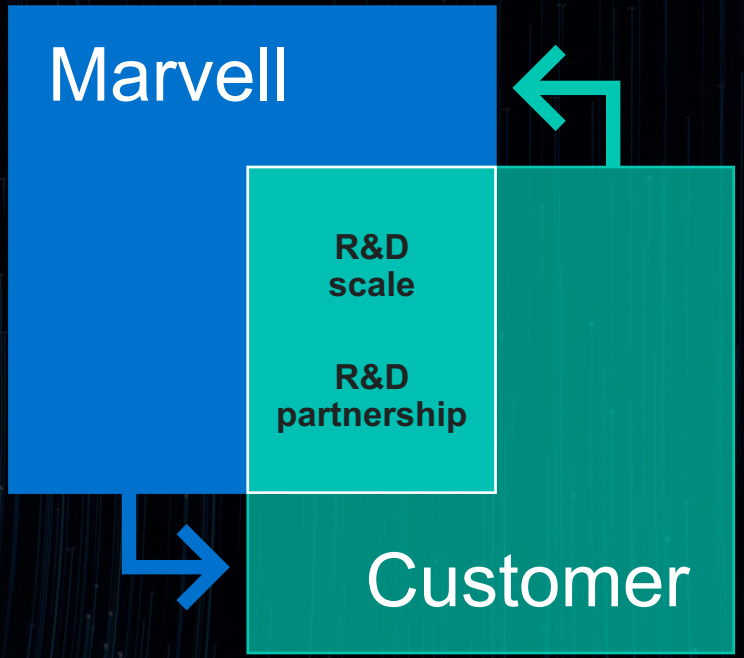
Customer C

AI accelerator

CY2026 ramp

AI compute: 3 out of 4 U.S. hyperscale operators

Investing for success



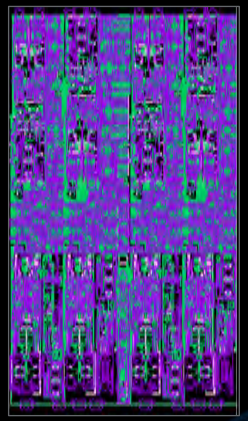
Partnering and co-investing with customers

Marvell accelerated infrastructure platform

Process node

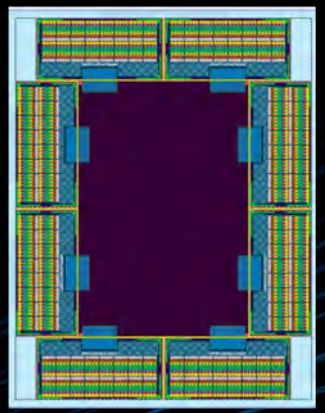
- 5nm
- 3nm
- 2nm

IP



SerDes

Packaging

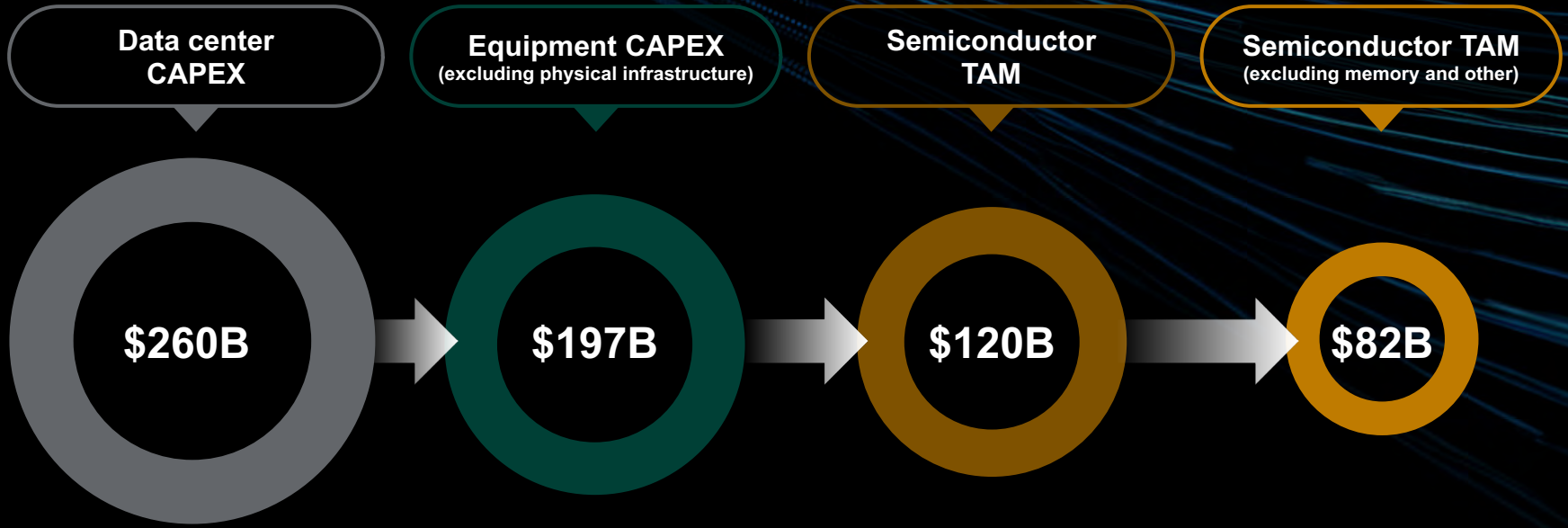


2.5D/3D

Expertise

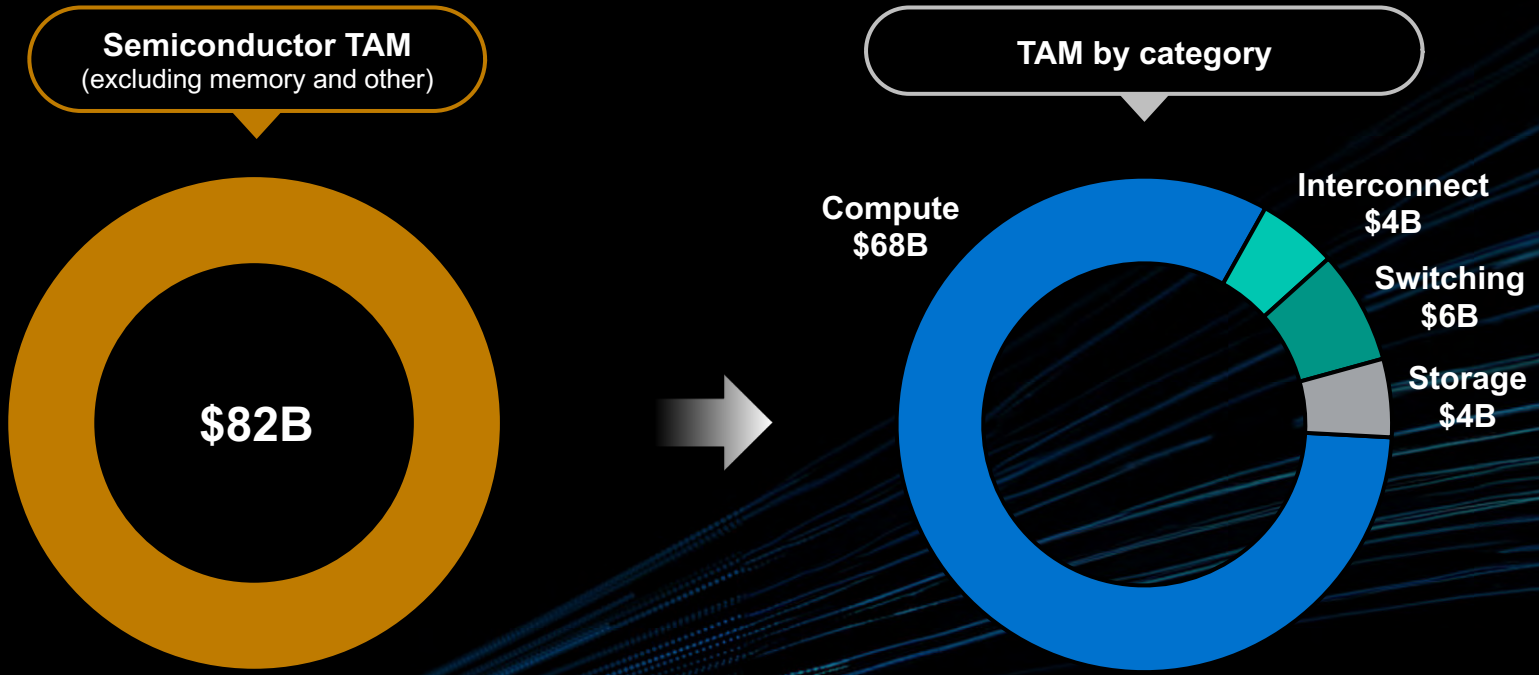
- Processor
- Large silicon
- Multi-chip
- Chiplet
- High bandwidth
- Networking
- SiPho

2023 data center infrastructure market



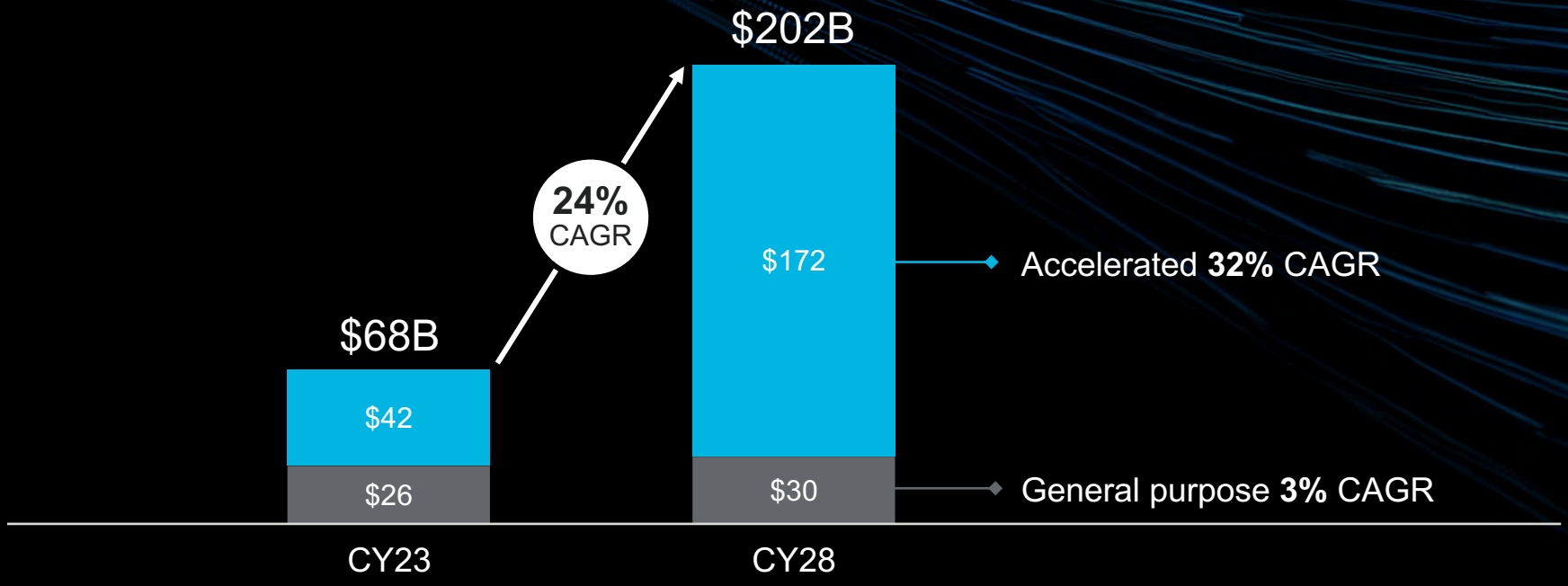
Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

2023 data center semiconductor TAM



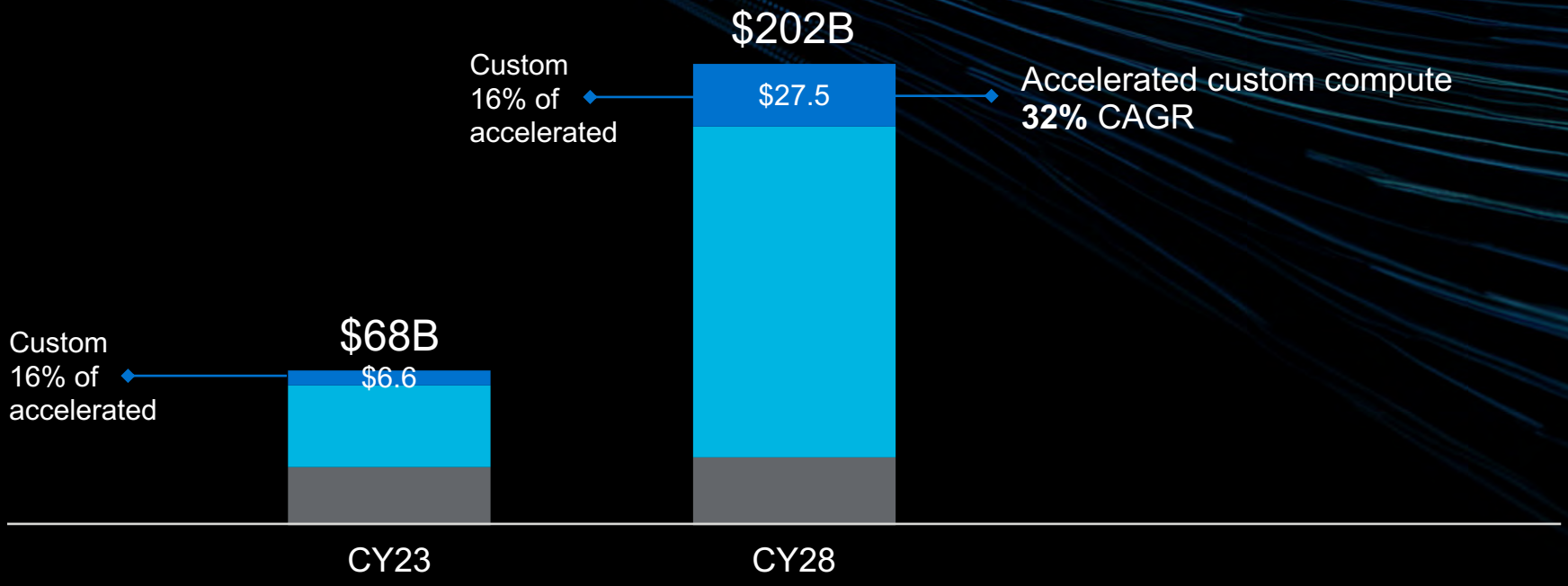
Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Data center **accelerated compute** opportunity



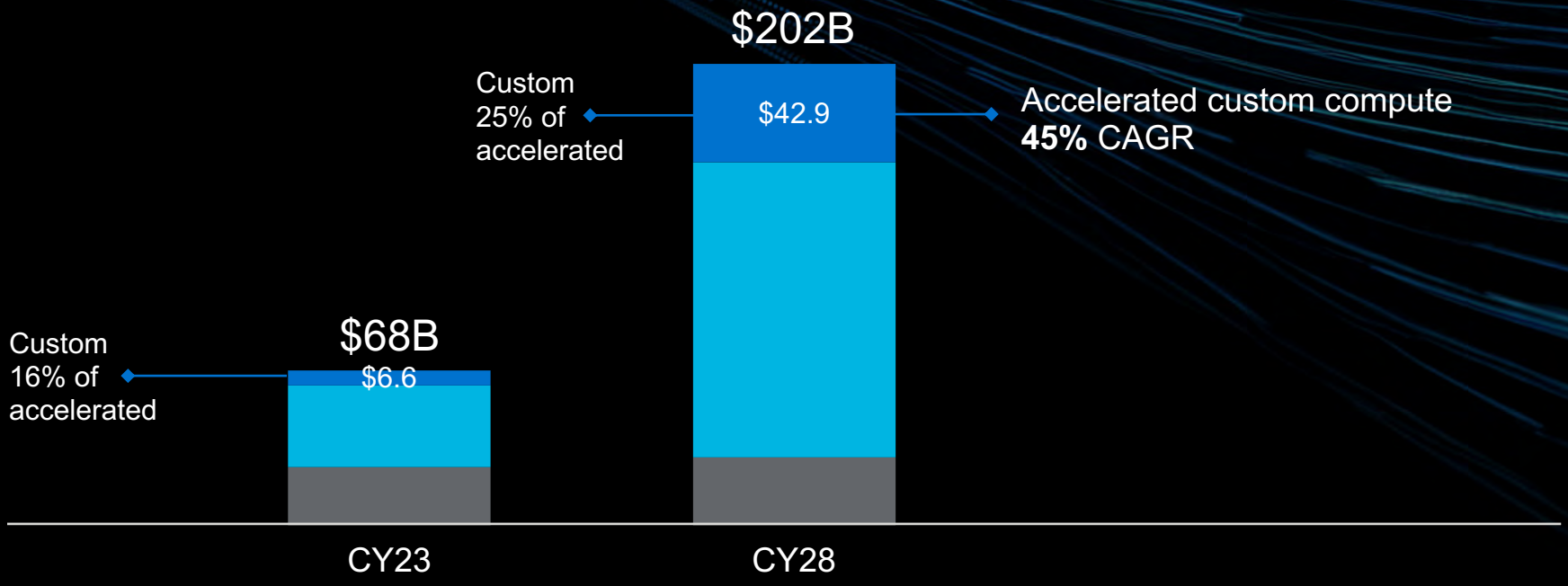
Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Data center **custom compute** opportunity



Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Data center **custom compute** opportunity



Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

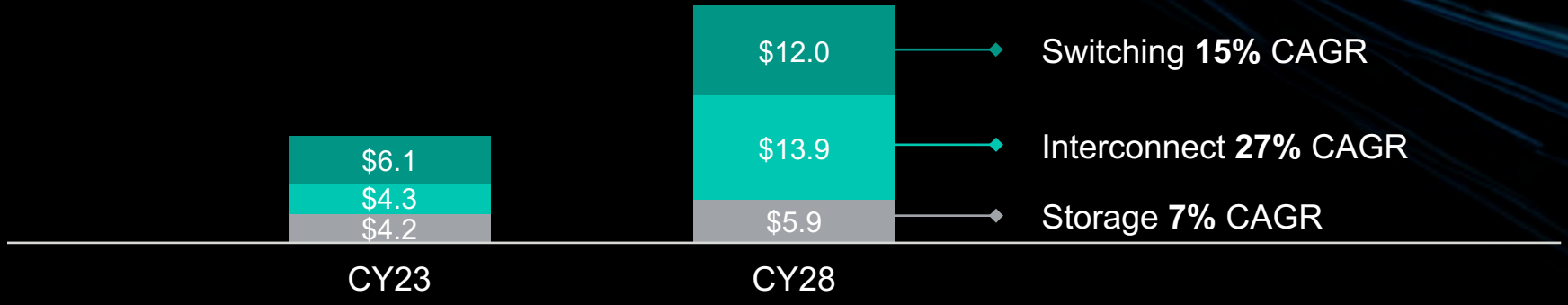
Data center **storage** opportunity

Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Data center **interconnect** opportunity

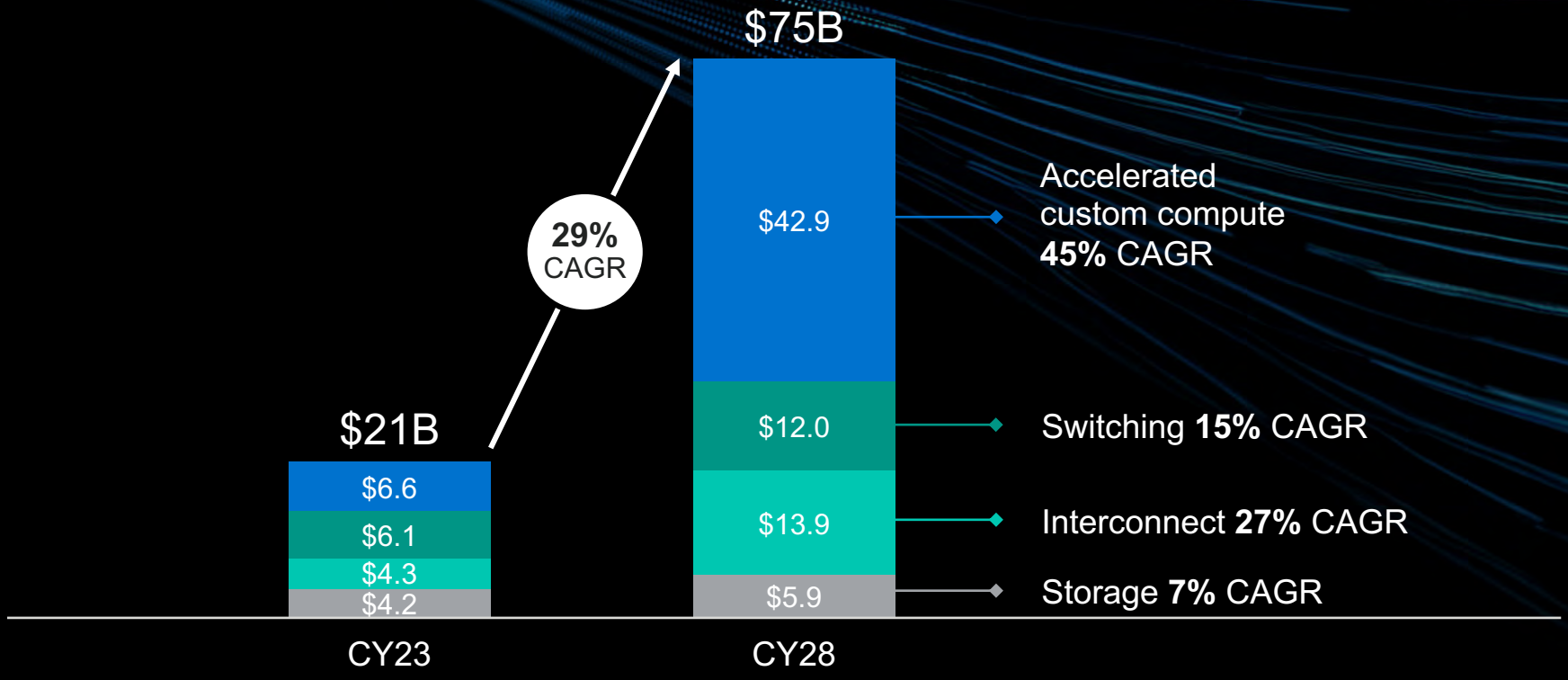
Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Data center **switching** opportunity



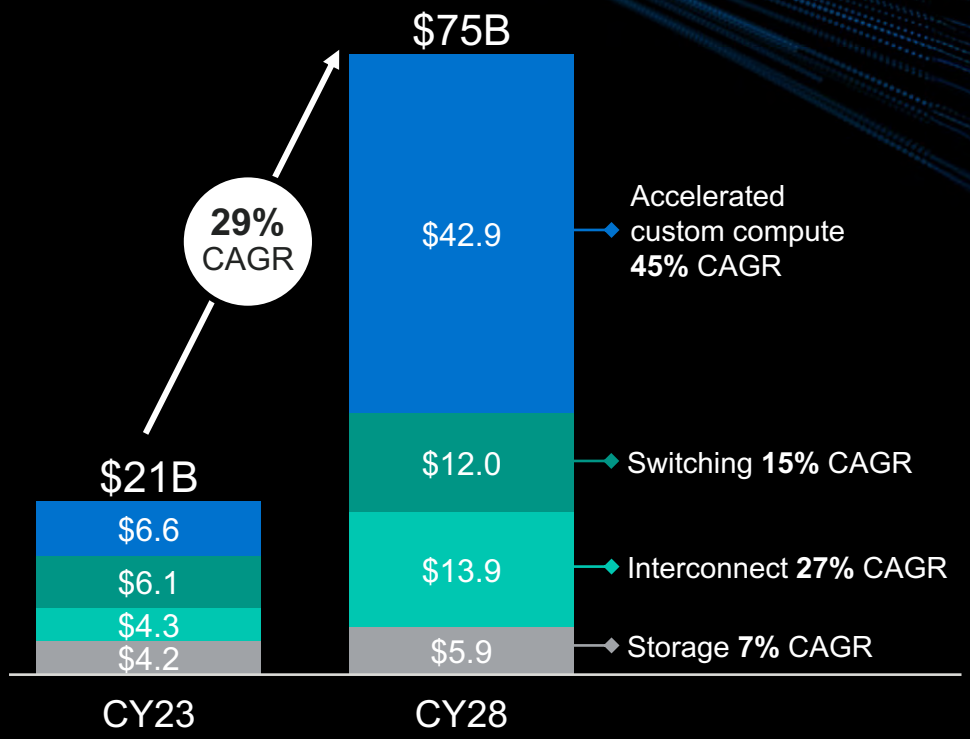
Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Marvell data center TAM



Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Fast growing market, expanding share



Last year: ~10% share

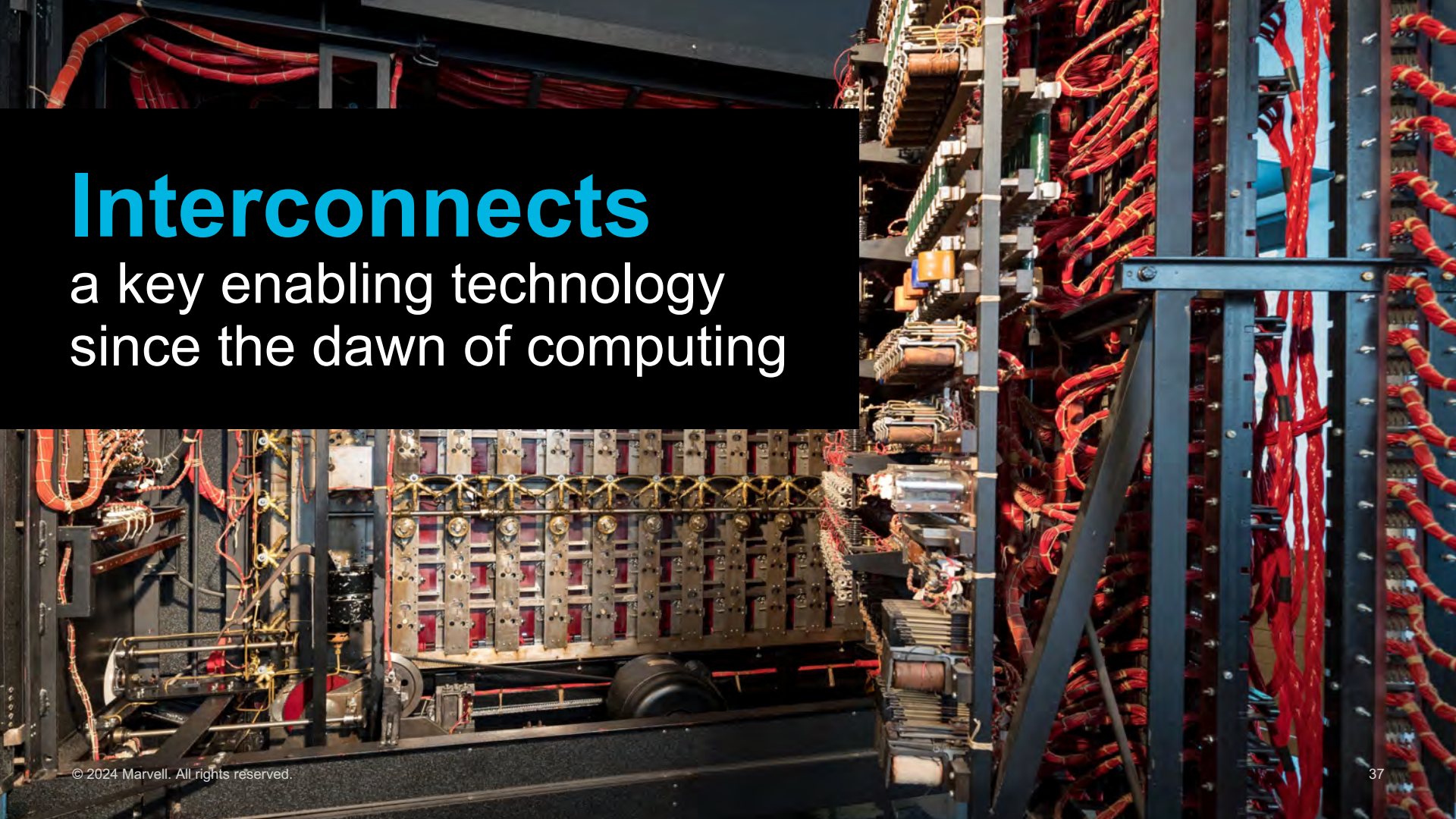
End-market	Share expectations
Accelerated custom compute	Gain
Switching	Gain
Interconnect	Maintain
Storage	Maintain

Long-term target: 20% share

Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Loi Nguyen

EVP and GM, Cloud Optics



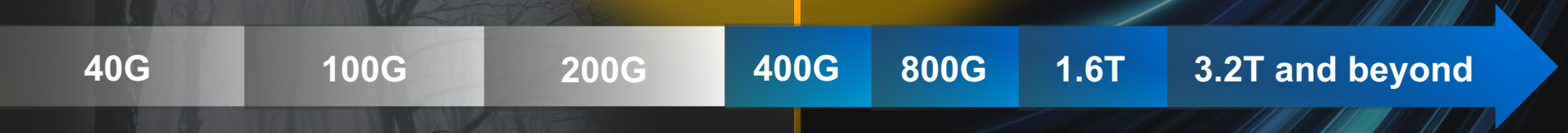
Interconnects

a key enabling technology
since the dawn of computing

A new beginning

AI

2023 = Year 0

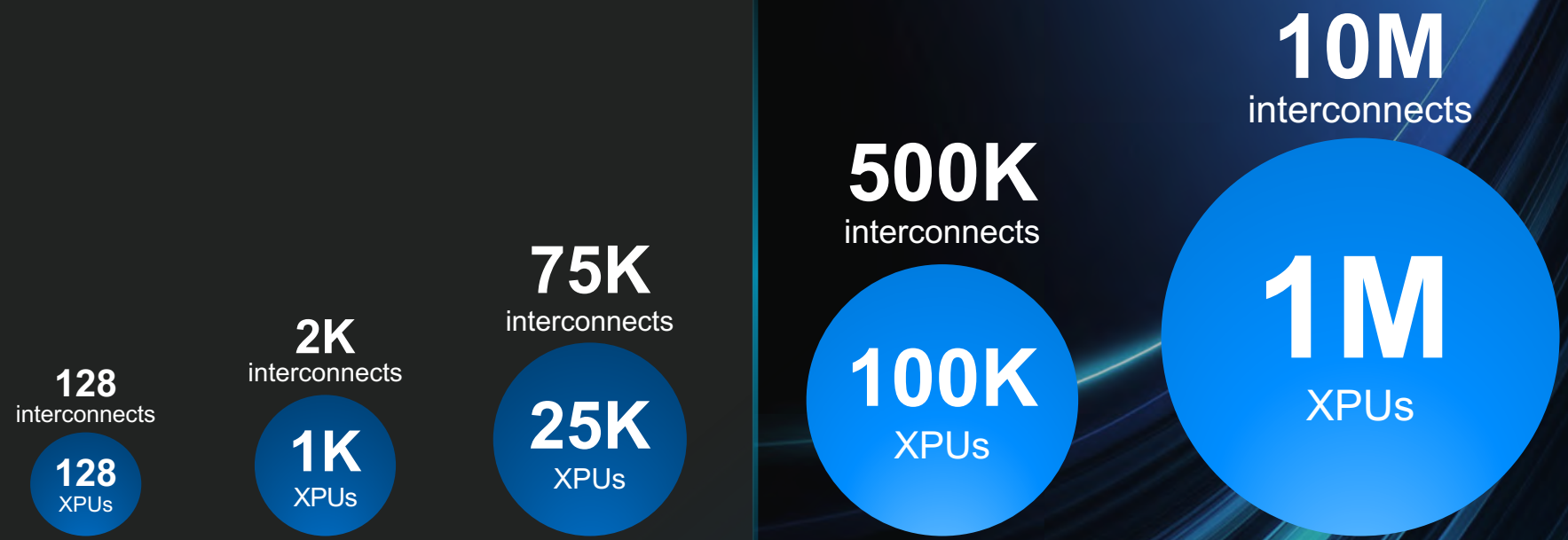


2X every **4** years

2X every **2** years

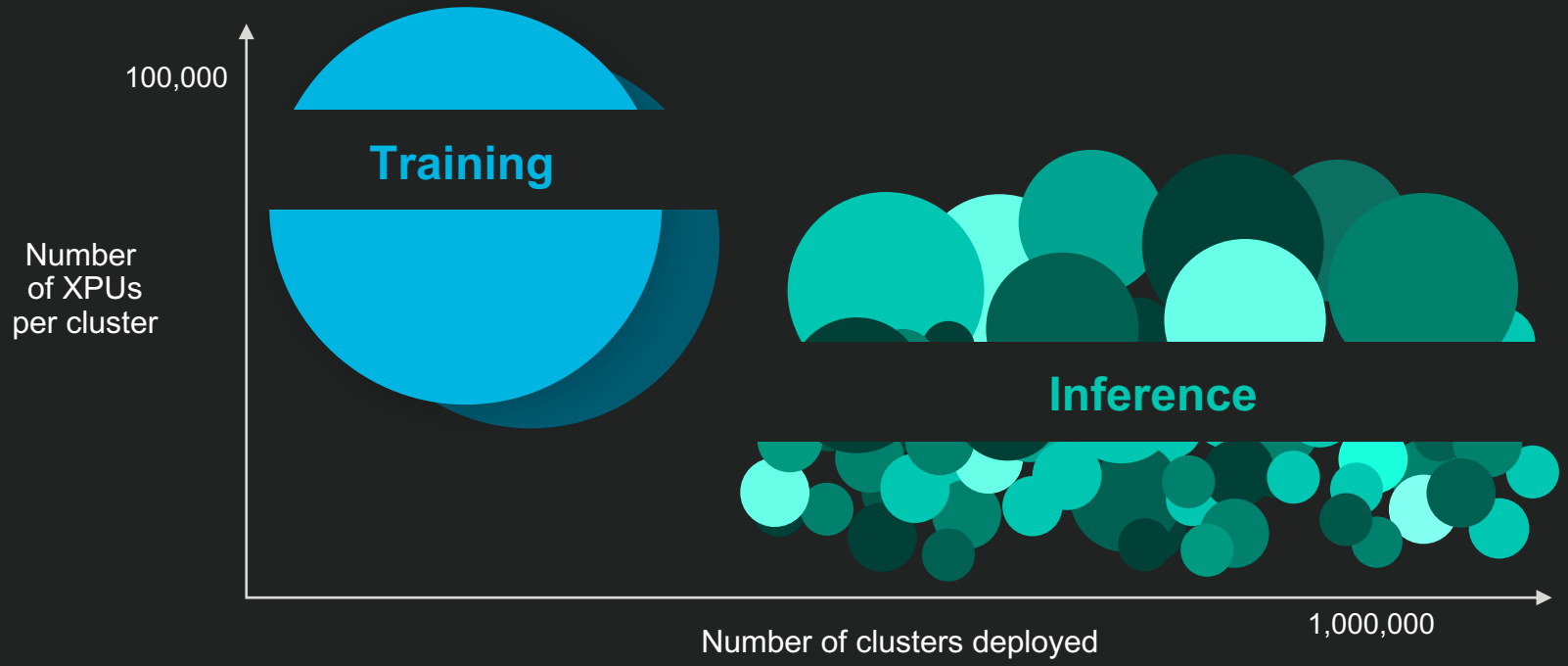
AI doubles interconnect speed in half the time

Optical interconnects enable large AI clusters



Optical interconnects growing faster than XPUs

Training vs Inference – what's the difference?



Both drive massive amount of interconnects

Need new infrastructure for AI

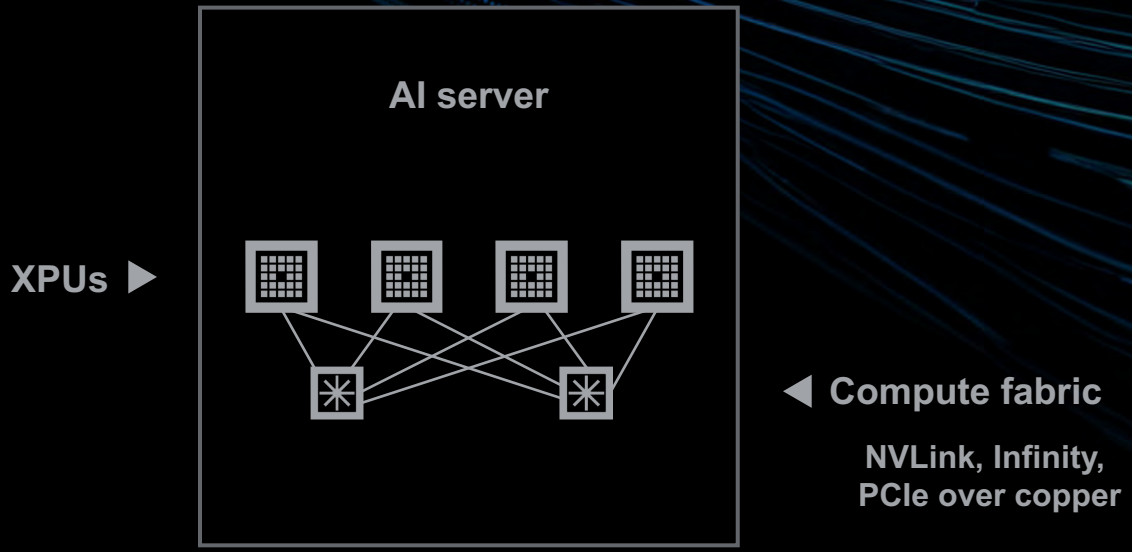
- More power
- Better cooling
- Within borders

More data centers, more locations, more interconnects

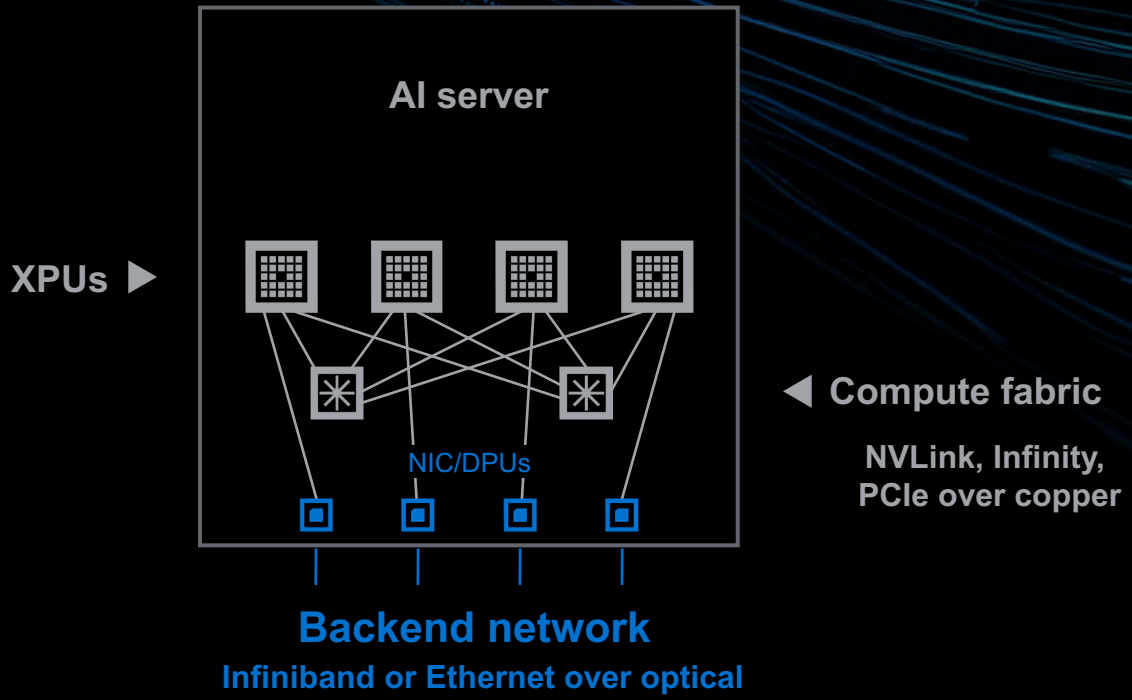
Source: datacentermap.com

Accelerated Infrastructure

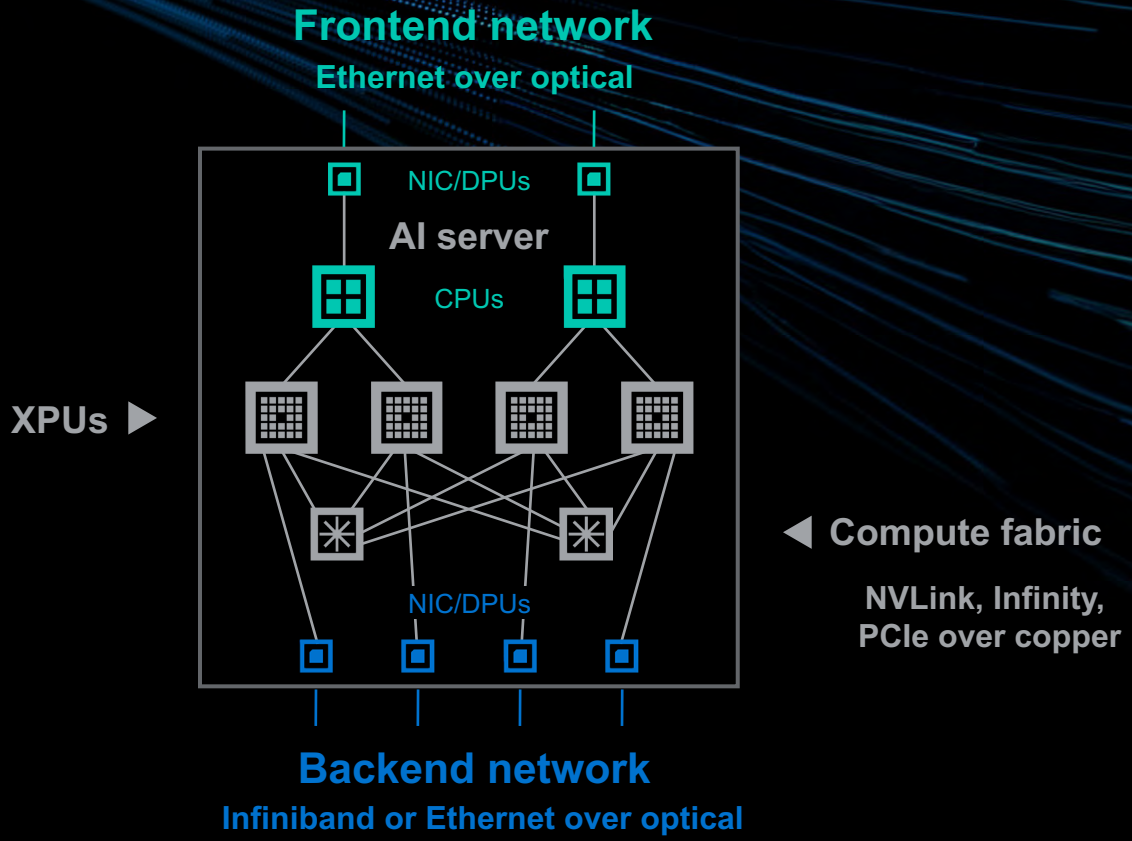
Compute fabric connects XPUs within a server



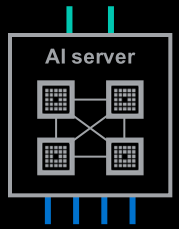
Backend network connects servers within a cluster



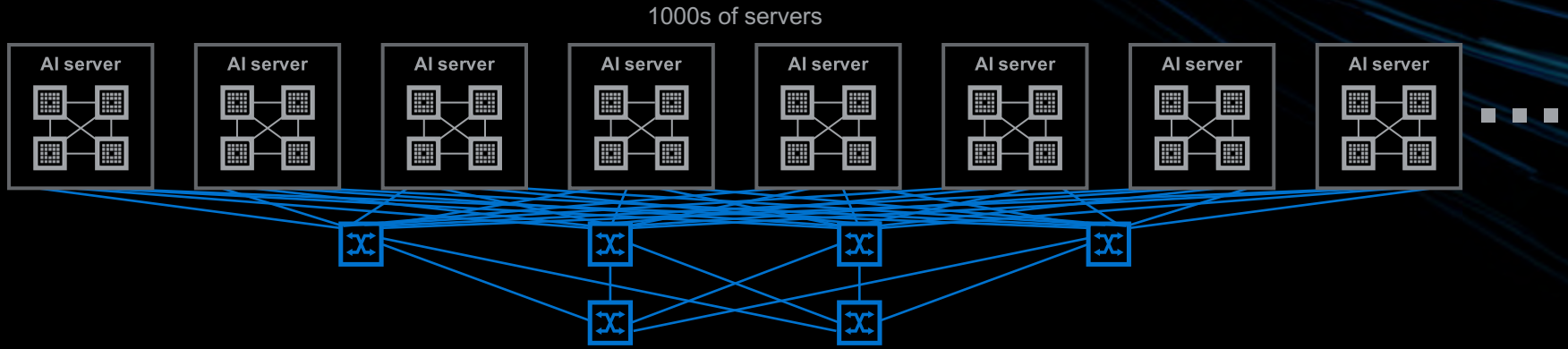
Frontend network connects servers to data center



AI cluster with **backend network**

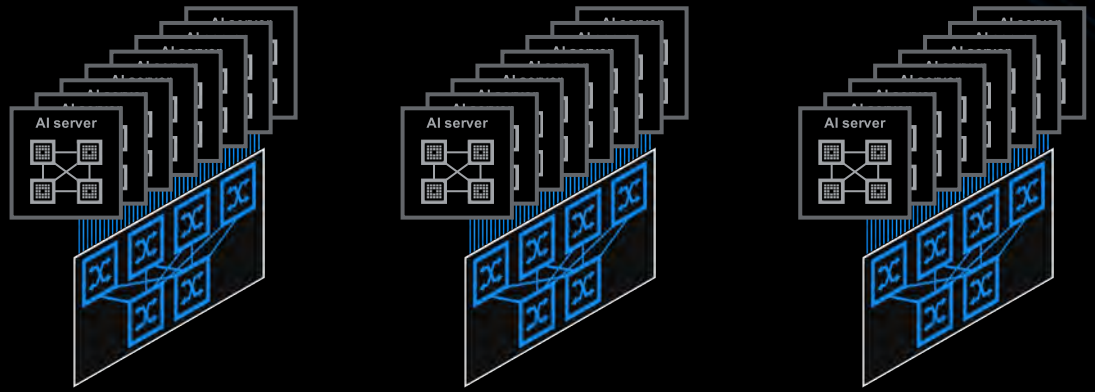


AI cluster with **backend network**



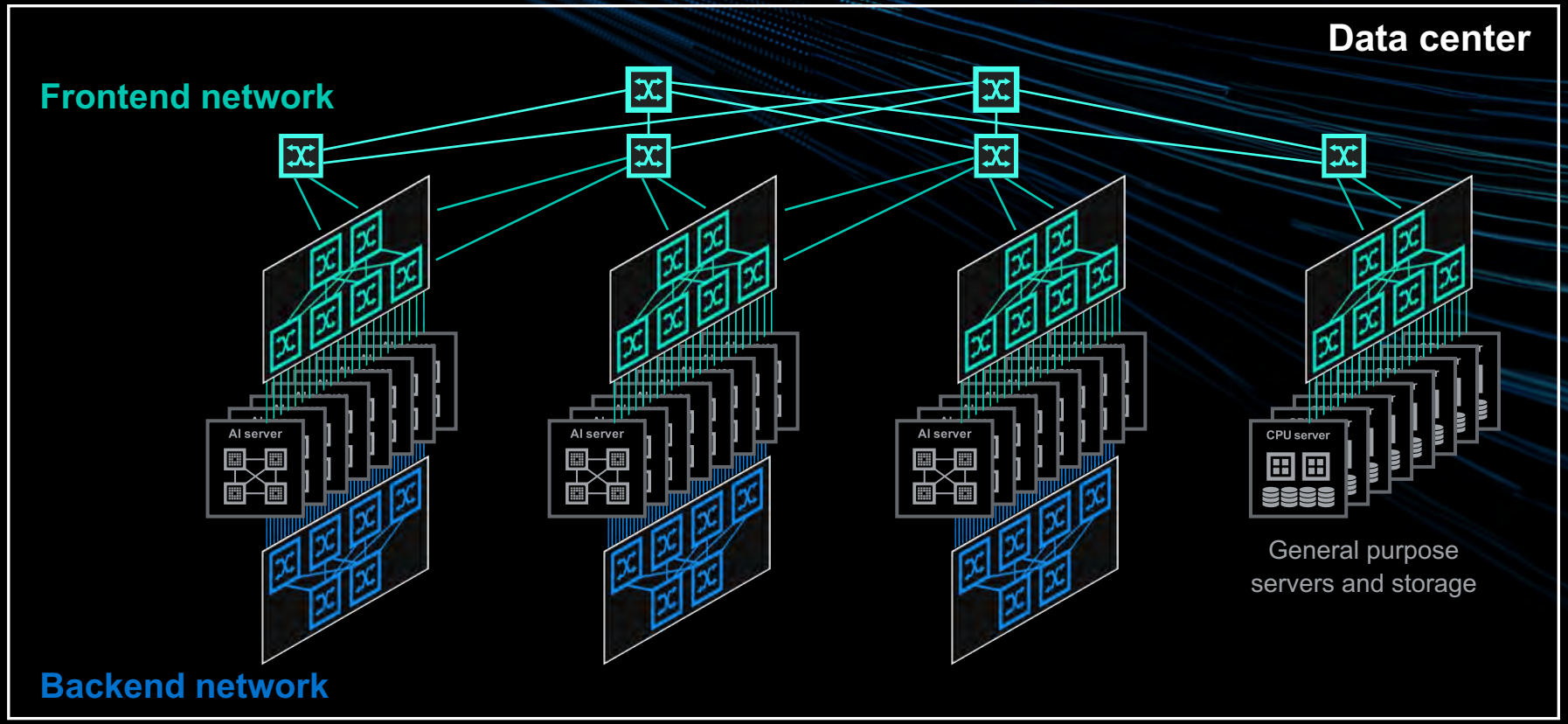
Backend network

AI clusters with **backend network**

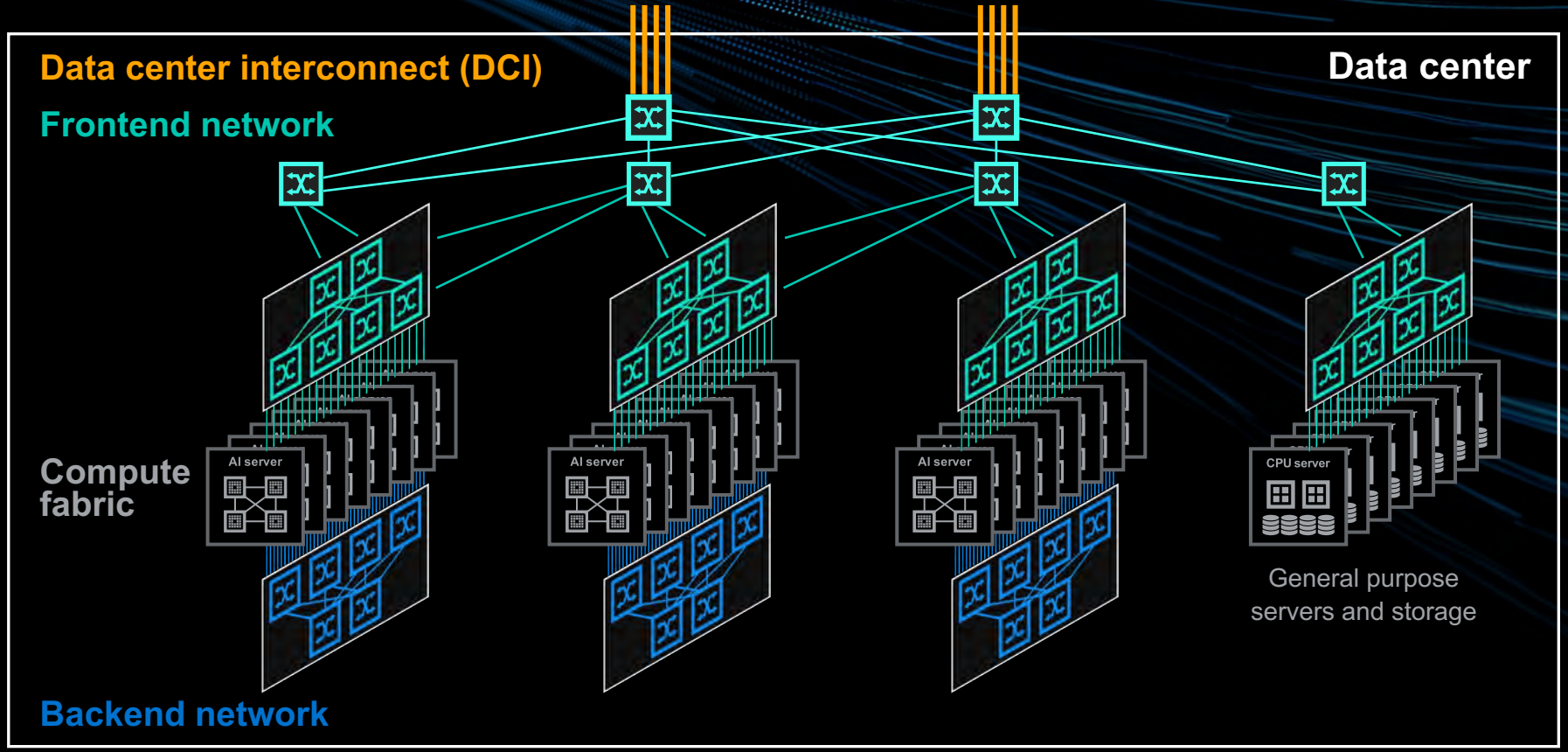


Backend network

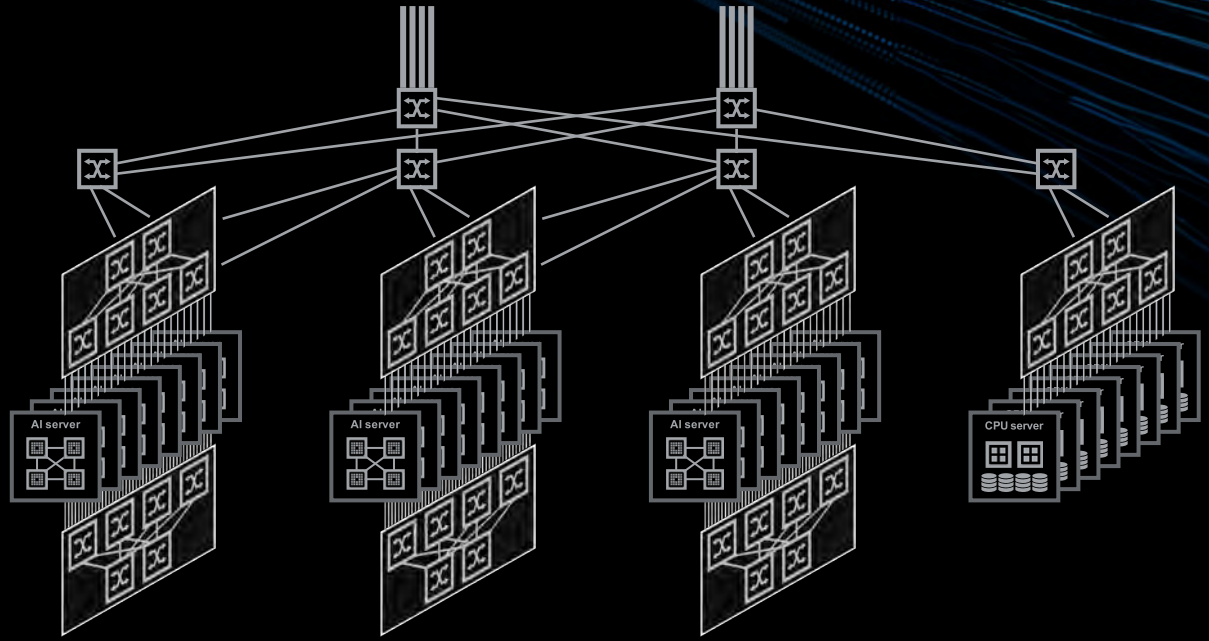
AI clusters with backend and frontend networks



DCI network connects data center to outside world

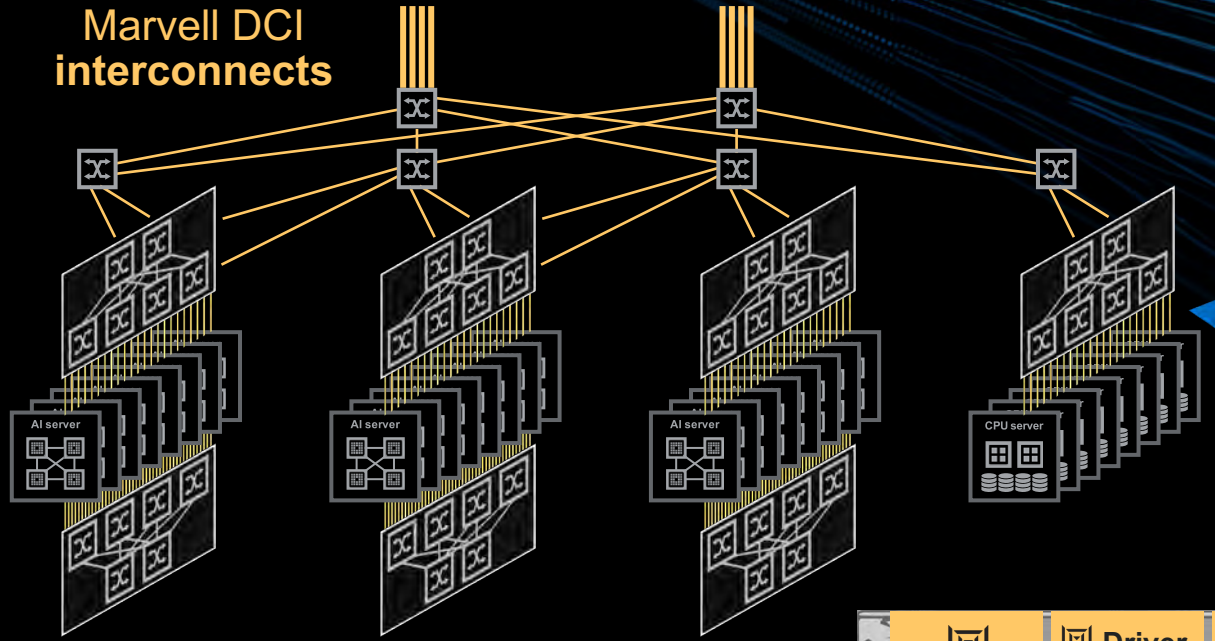


Marvell accelerated infrastructure silicon TAM

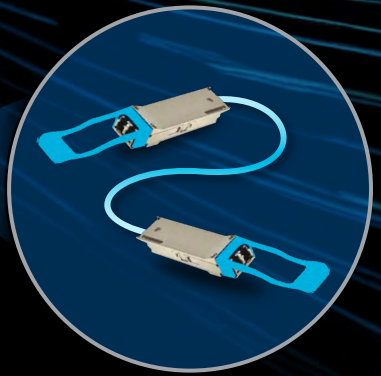


Marvell accelerated infrastructure silicon TAM

Marvell DCI **interconnects**

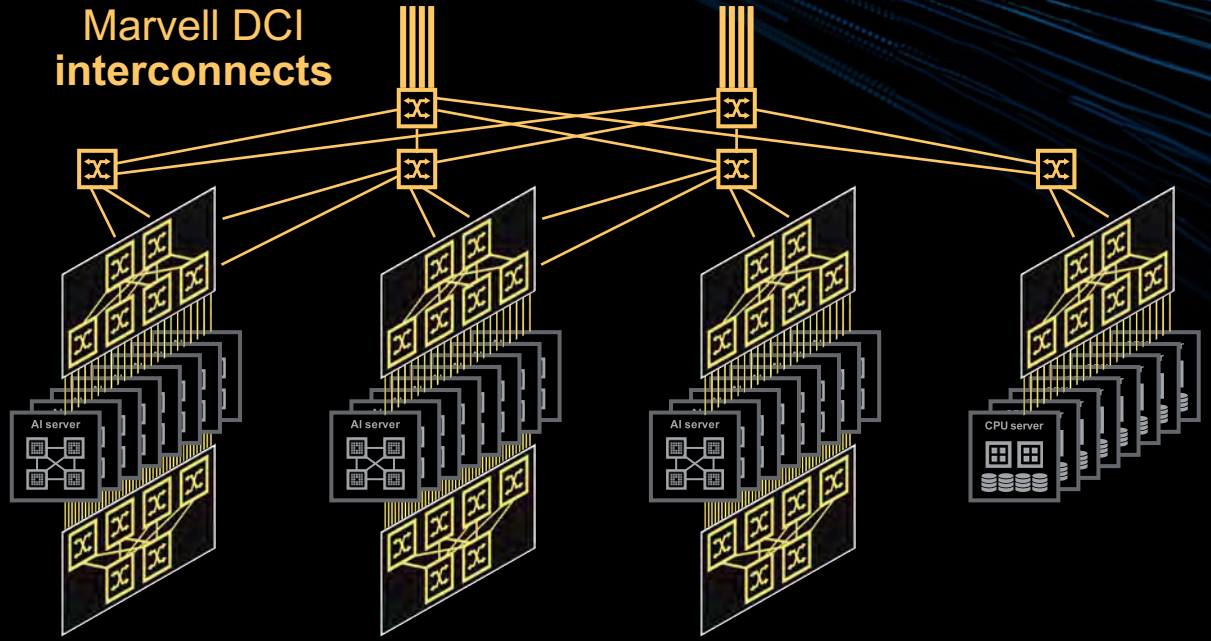


Optical interconnects

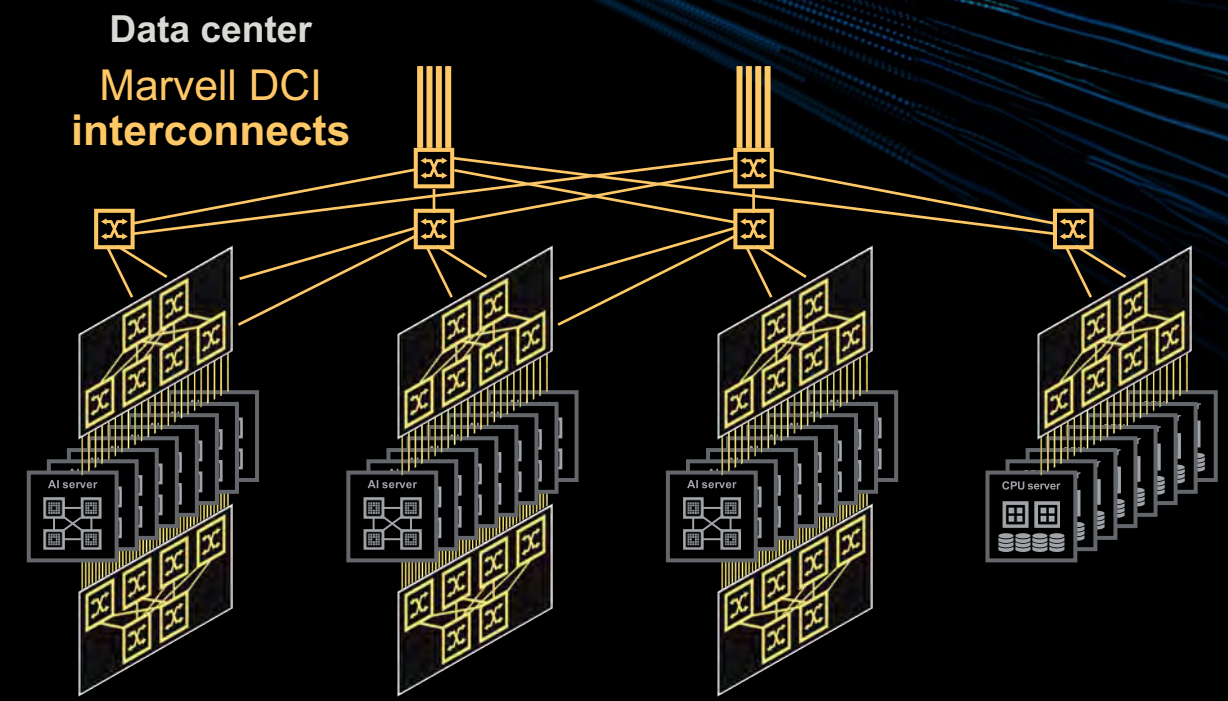


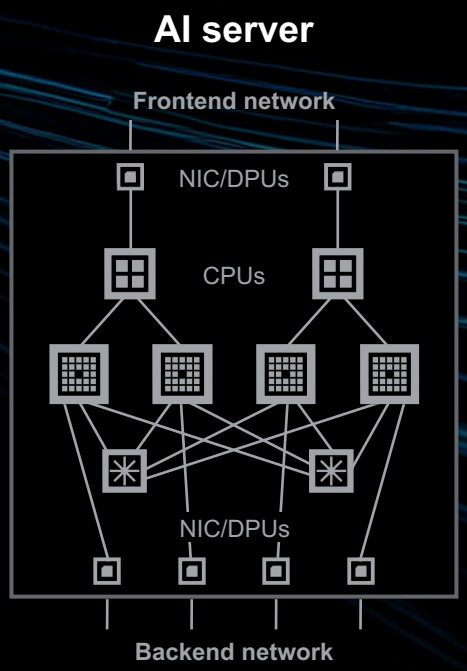
Marvell inside data center **interconnects**

Marvell accelerated infrastructure silicon TAM



Marvell accelerated infrastructure silicon TAM

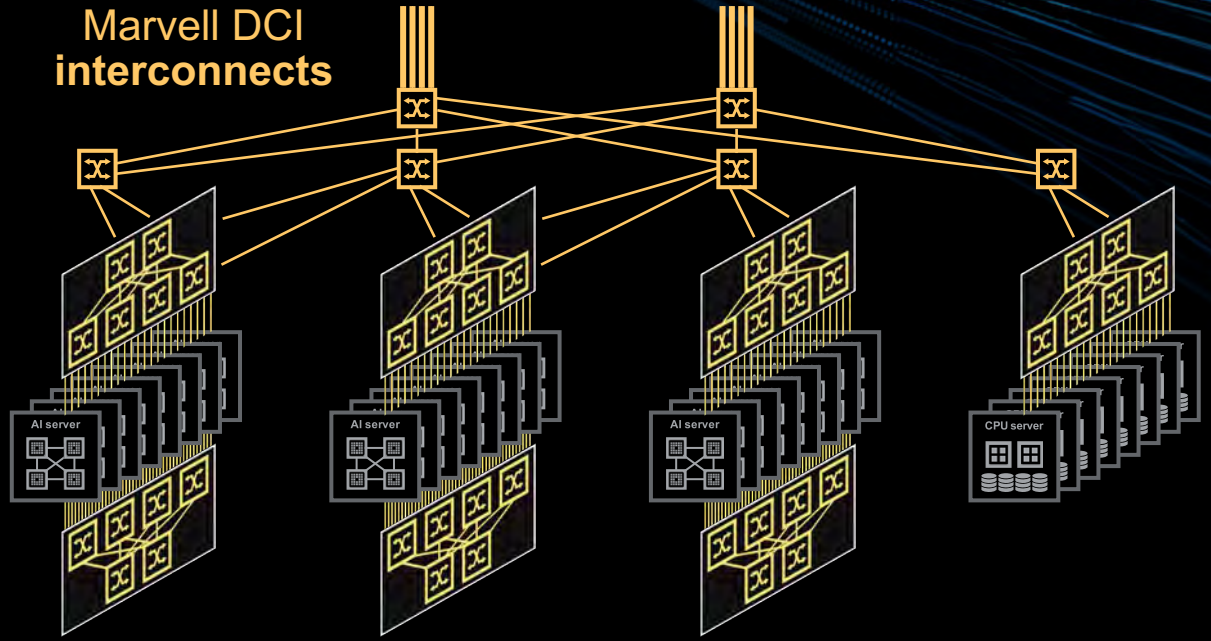




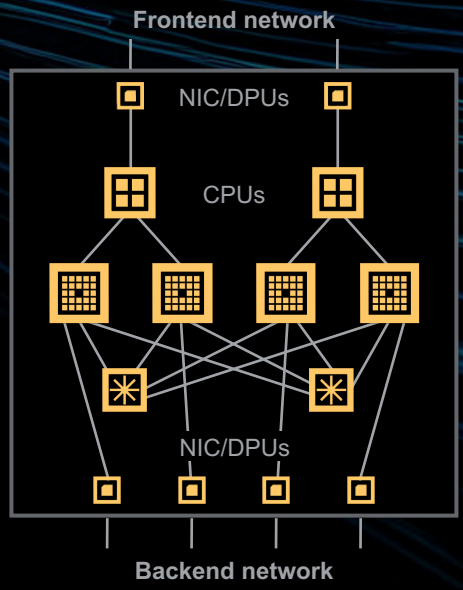
Marvell accelerated infrastructure silicon TAM

Data center

Marvell DCI **interconnects**



AI server



Marvell inside data center **interconnects**

Marvell **switching**

Marvell **custom compute**

Achyut Shah

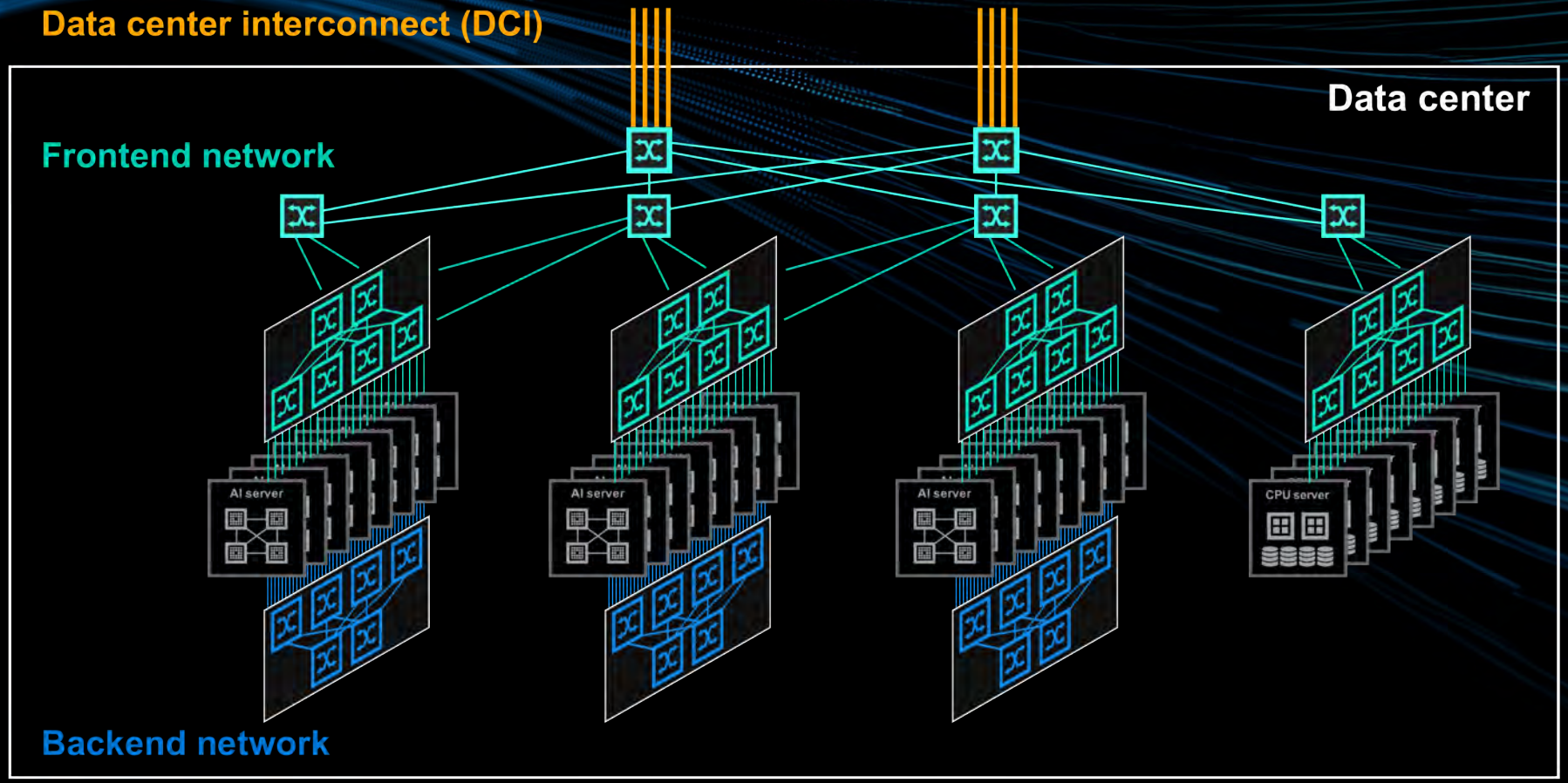
SVP and GM, Connectivity

Achyut Shah

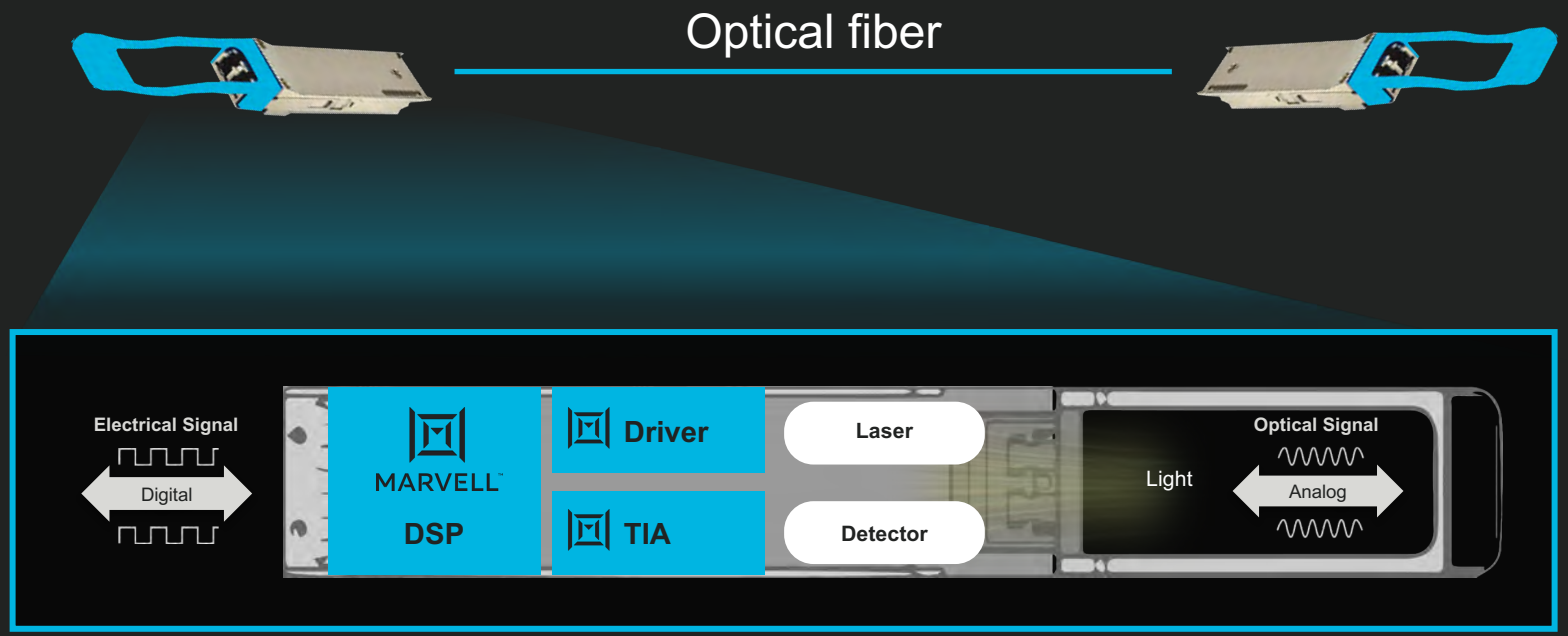
SVP and GM, Connectivity

Maxim, VP and GM
Cloud and Data Center BU
1998 – 2020

BSEE, MBA
Michigan Tech University
Santa Clara University



What's inside an **optical** interconnect module?



Technology leadership at scale

Leading node digital

- PAM IP
- Coherent IP
- Signal processing
- Forward error correction

High frequency analog

- SiGe TIA
- SiGe driver
- CMOS TIA
- CMOS driver

System level IP

- Diagnostics
- Telemetry
- Firmware
- Software

Deep customer partnerships, complete IP upgrade every 2 years

Inside
data centers

Frontend network
Backend network

Multi-generational **leadership** in PAM platform

First PAM DSP

200G

4 x 50G

First 100G per lane

400G

4 x 100G

Enabled **AI ramp**

800G

8 x 100G

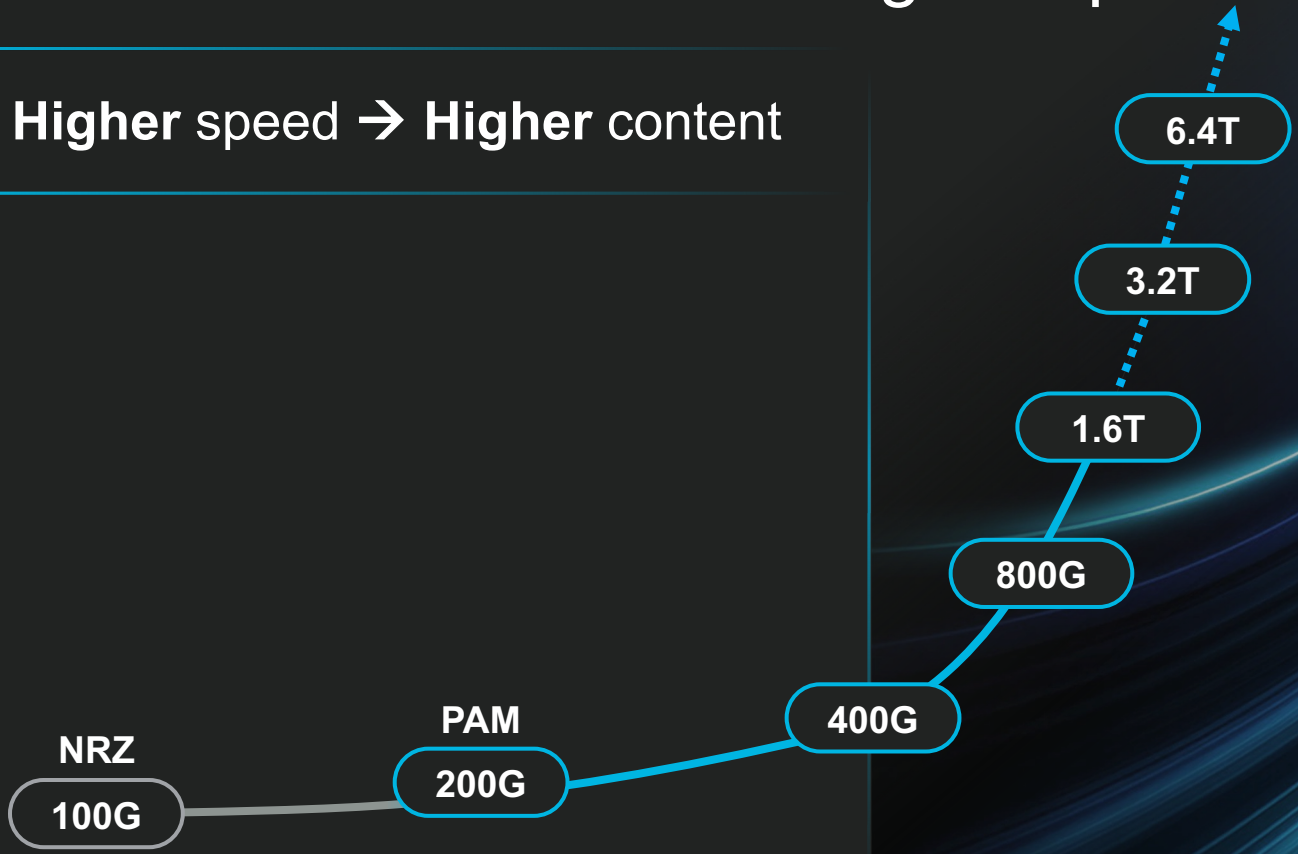
First 200G per lane

1.6T

8 x 200G

AI **accelerates** need for higher speed

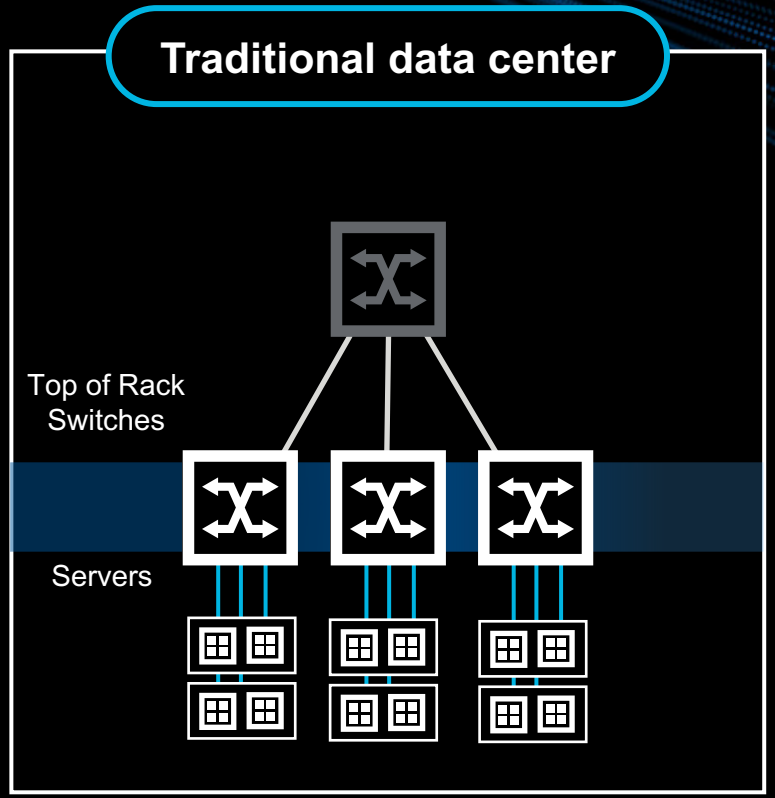
Higher speed → **Higher** content

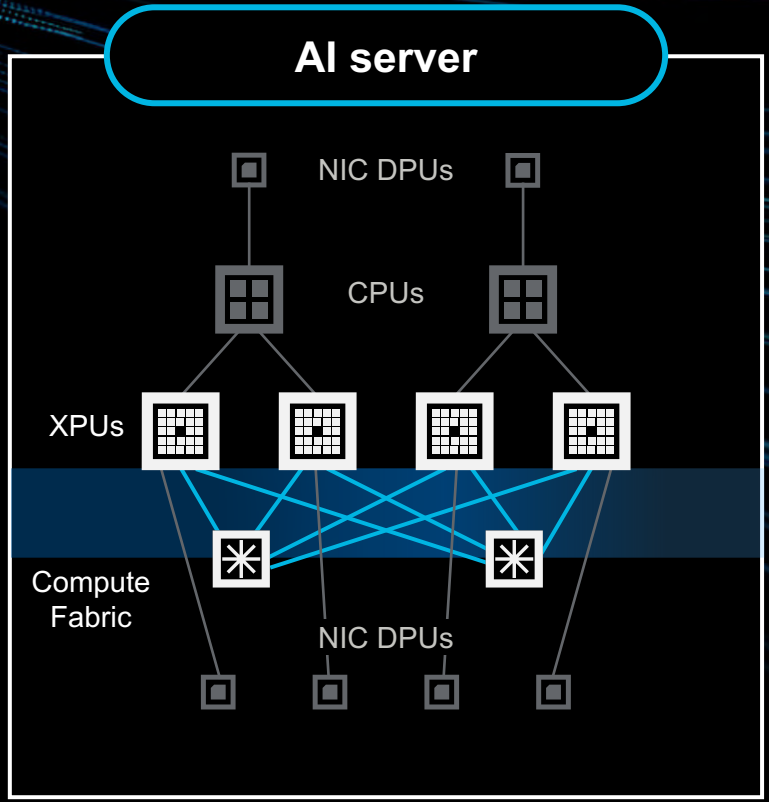


New opportunity

Active Electrical PAM DSPs

Where are copper interconnects used?





Higher speeds drive need for **active interconnects**

AEC PAM DSPs
Active Electrical Copper

Go to market

Cable partners

Amphenol · TE connectivity · molex · BROADEX · 3M · eoptolink · BizLink · ZHAOLONG · FIT · LUXSHARE ICT · Volex

Scalable ecosystem

New
$1B
DSP TAM

Shipping now to hyperscale customers

Between data centers

Data center interconnect (DCI)

Multi-generational **leadership** in DCI platform

MARVELL Coherent DSP

MARVELL Driver

MARVELL TIA

MARVELL SiPho

COLORZ® 100

First DCI pluggable

COLORZ® 400

First **Coherent** DCI pluggable

COLORZ® 800

First 800G **Coherent** pluggable

DCI TAM expansion

Current DCI market

120 kilometers

pluggable

Market opportunity **doubling**

Marvell COLORZ® 400 / 800

New DCI opportunity

1,000 kilometers

Transport box

transition to **pluggable**

Marvell COLORZ® 800 with **PCS**
probalistic constellation shaping

New **$1B** DCI TAM

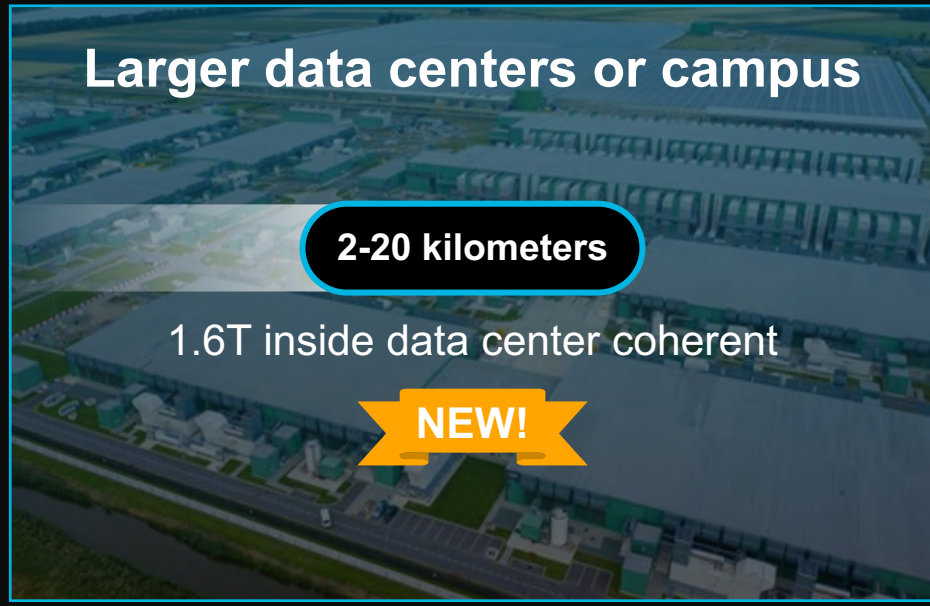
Larger AI clusters require **new interconnect**

Inside data center

<2 kilometers

1.6T PAM

Larger data centers or campus



2-20 kilometers

1.6T inside data center coherent

NEW!

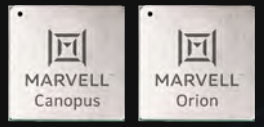
Marvell inside data center coherent sampling 2H CY24

Complete interconnect portfolio

Highest speed PAM4 DSPs

Drivers, TIAs

SiPho

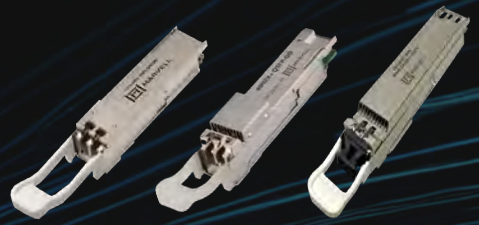


Highest speed coherent DSPs

AEC DSP

Integrated DSPs

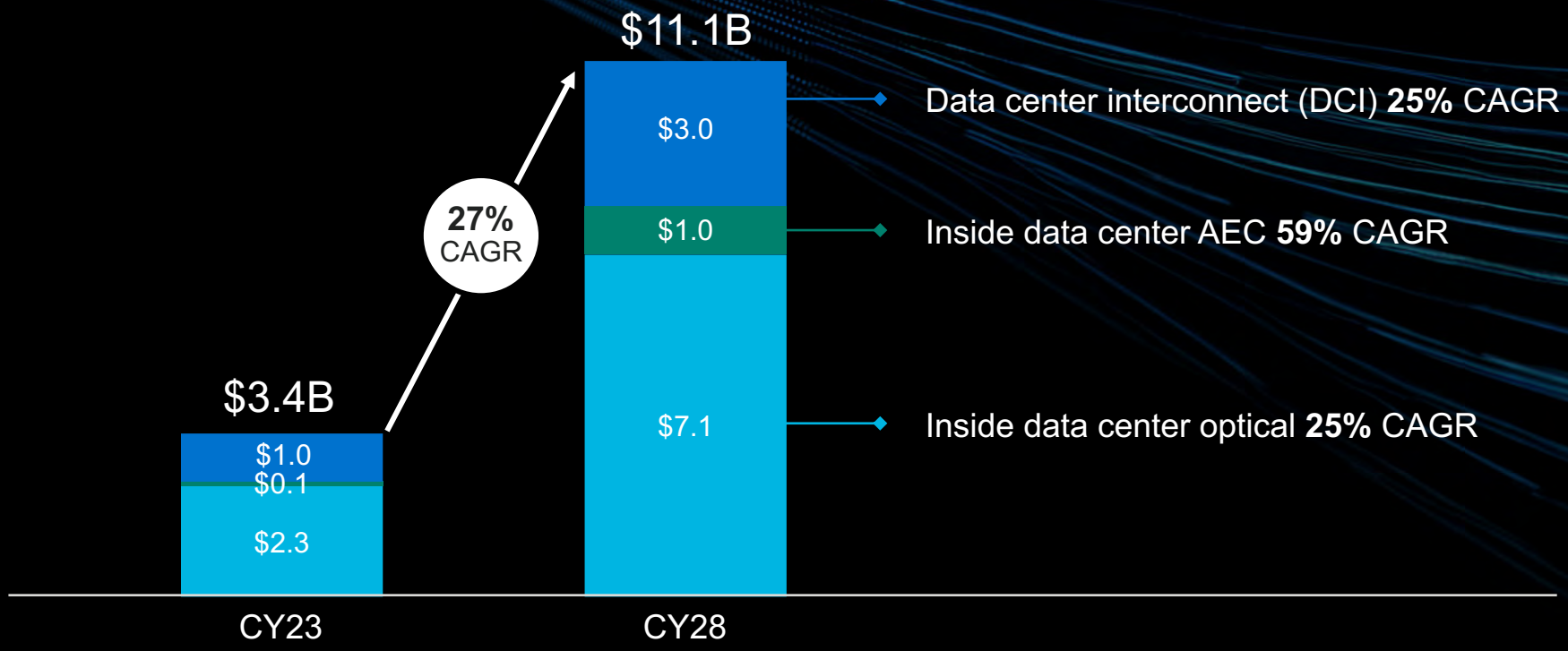
Inside data center coherent



COLORZ® DCI modules

200G to 1.6T and beyond, 1 meter to 1,000 kilometers

Marvell **interconnect** TAM

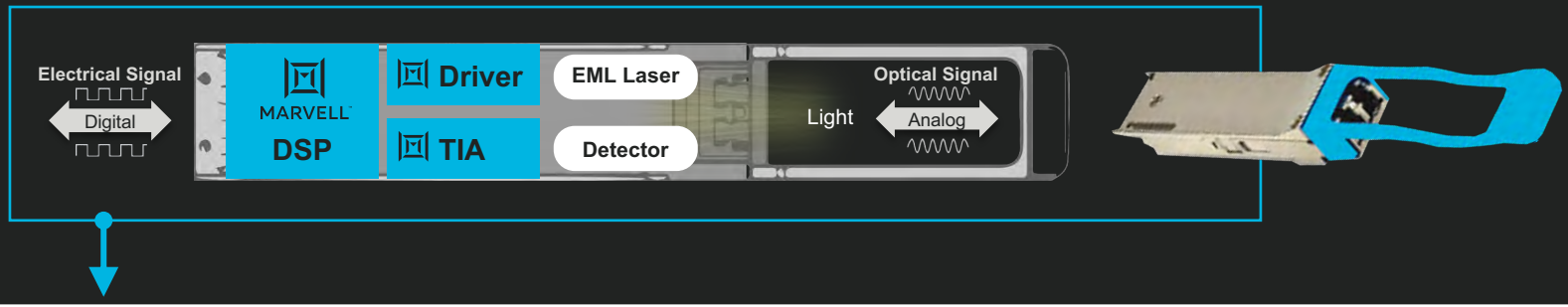


Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Loi Nguyen

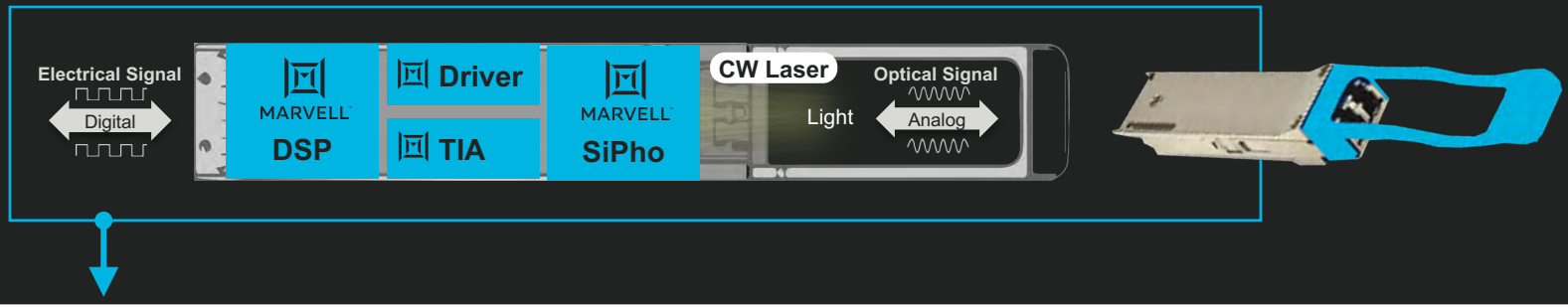
EVP and GM, Cloud Optics

What's inside an **optical** module?



DSP	SerDes, error correction, telemetry, gearbox, interoperability
Driver	Amplifies electrical signal from DSP to drive laser
TIA	(Transimpedance amplifier) Amplifies electrical signal from detector
EML Laser	(Electron-absorption modulator laser) High-speed laser
Detector	High-speed photo detector

What's inside **silicon photonics** module?



DSP	SerDes, error correction, telemetry, gearbox, interoperability
Driver	Amplifies electrical signal from DSP to drive laser
TIA	(Transimpedance amplifier) Amplifies electrical signal from detector
SiPho	(Silicon Photonics) converts electrical signal to light and vice versa
CW Laser	Continuous wave (CW) laser source

Marvell **SiPho** products shipping in volume

COLORZ® 100

First DCI pluggable

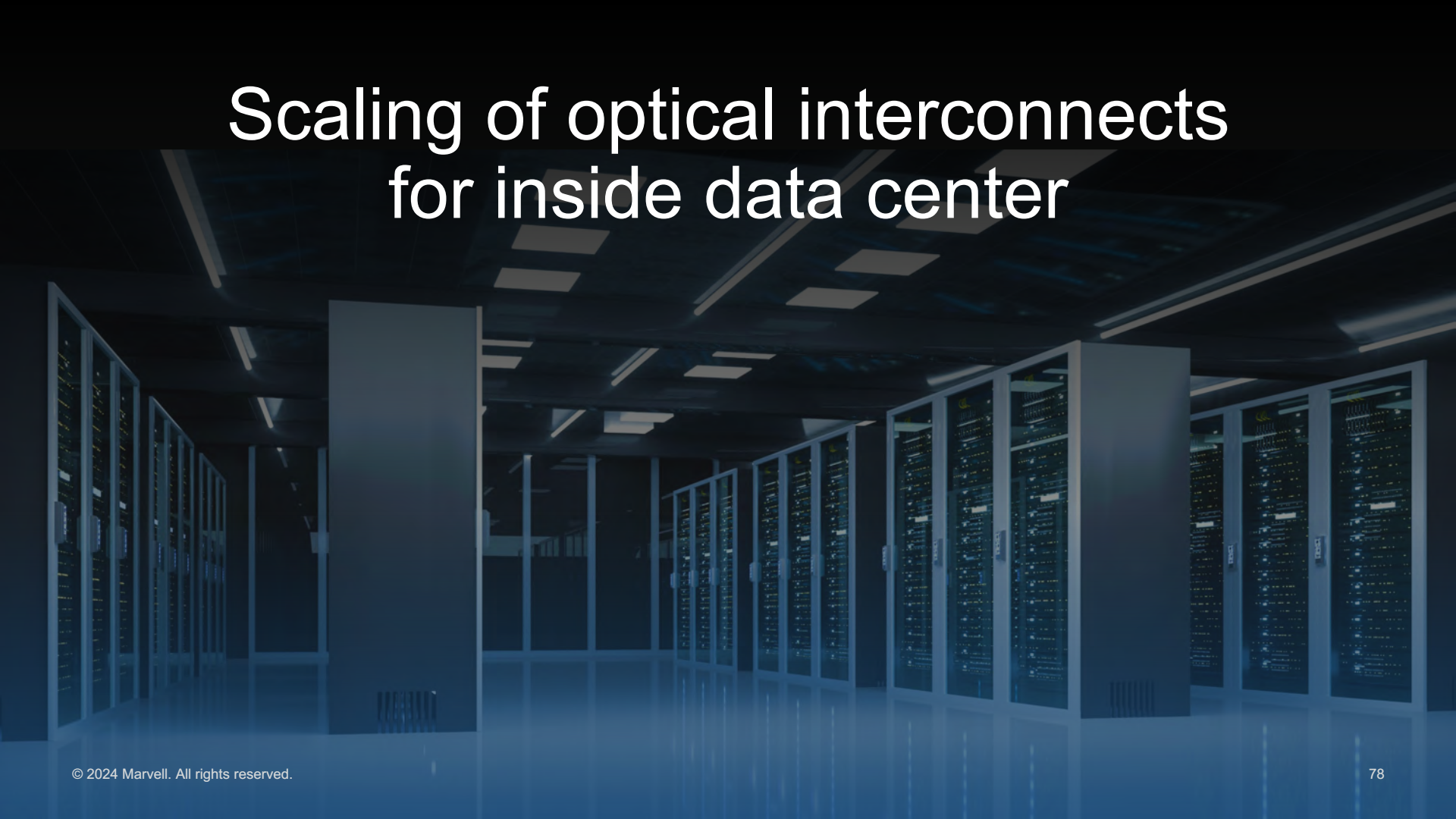
COLORZ® 400

First **Coherent** DCI pluggable

COLORZ® 800

First 800G **Coherent** pluggable

Scaling of optical interconnects for inside data center



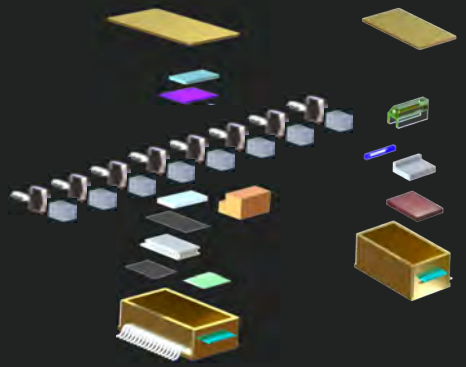
Discrete vs SiPho (1.6T pluggable)

Discrete

Components

8X

High-speed lasers, detectors



1X

DSP

SiPho

Silicon photonics + CW laser

2X

CW lasers

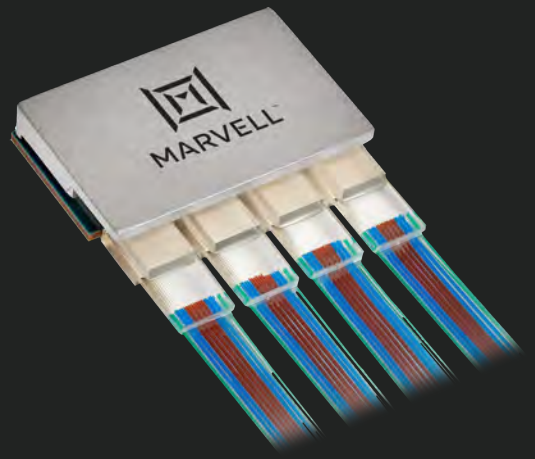
1X

SiPho

1X

DSP

Marvell 3D SiPho engine



NEW!

32 x 200G electrical and optical

100s components on chip

Modulators, photodetectors, couplers, MUX, DEMUX, capacitors, resistors

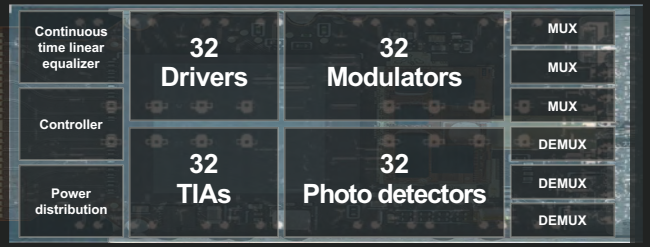
3D integration TIAs and drivers

Scalable 1.6T to 6.4T and more

4X bandwidth, lower cost per bit vs discrete

Marvell 3D SiPho engine

200G x 32 electrical line



200G x 32 optical line

Key terms

Modulator: converts electrical to light
Photo detector: converts light to electrical
Couplers: couples light waves
Multiplexer (MUX): combines wavelengths
Demultiplexer (DEMUX): separates wavelengths

NEW!

32 x 200G electrical and optical

100s components on chip
Modulators, photodetectors, couplers, MUX, DEMUX, capacitors, resistors

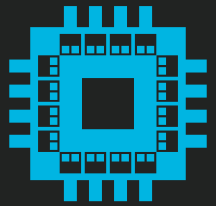
3D integration TIAs and drivers

Scalable 1.6T to 6.4T and more

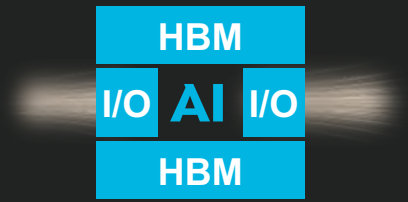
4X bandwidth, lower cost per bit vs discrete

3D SiPho engine multiple use cases

Inside pluggable
Next year



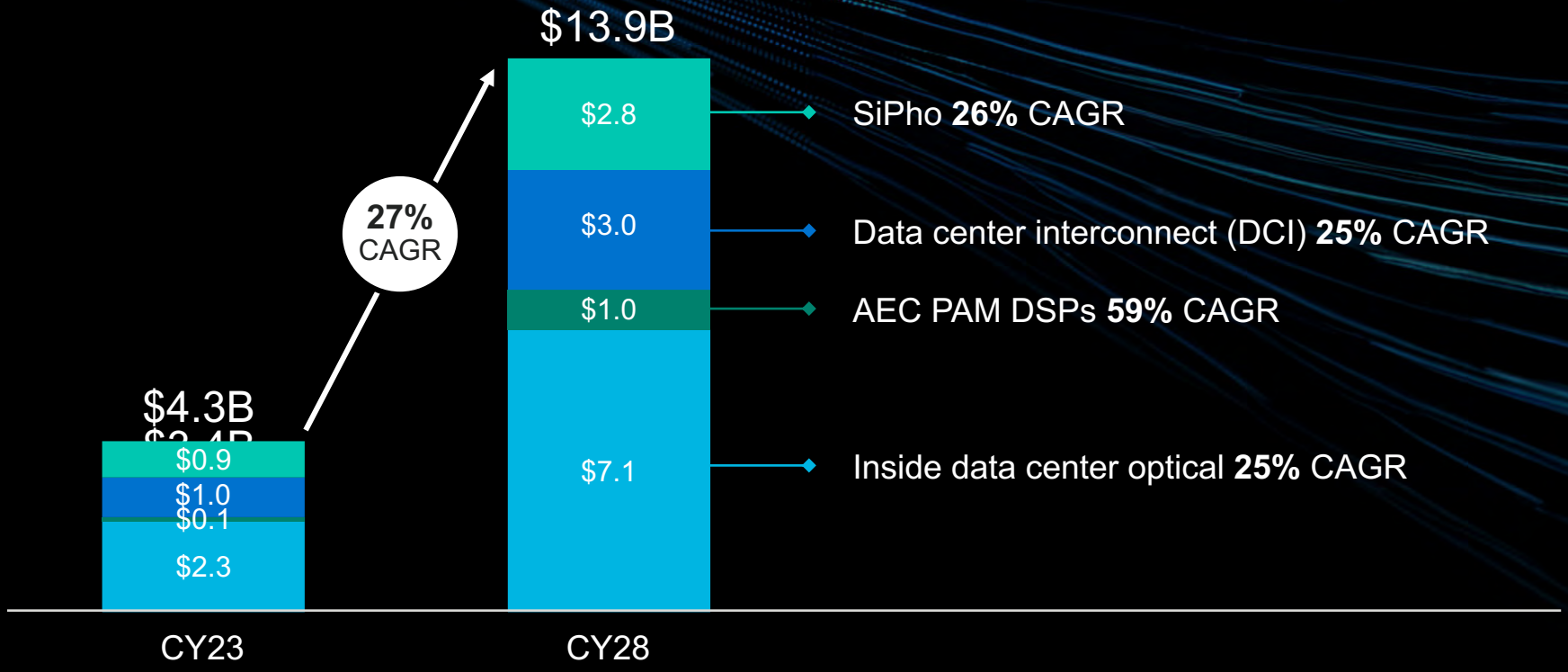
Co-packaged optics
Future



Optical chiplets
Future

Building blocks for scaling of optics

Marvell **interconnect** TAM



Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Nick Kucharewski

SVP and GM, Network Switching

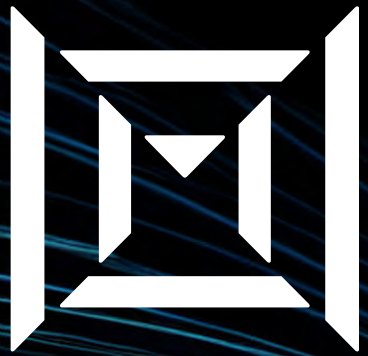
Nick Kucharewski

SVP and GM,
Network Switching

Qualcomm, SVP and GM
Wireless Infrastructure and Networking BU
2018 – 2023

Broadcom, VP of Product
Core Switching Group
2005 – 2017

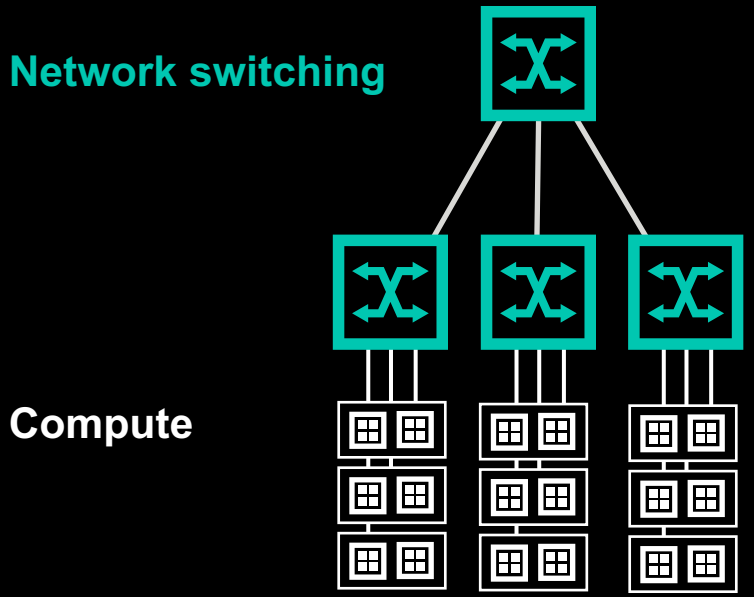
Stanford University
Electrical Engineering
B.S. and M.S.



Network Switching

- Market expansion
- Demonstrated capability to deliver
- Opportunities for product innovation
- Essential portfolio technology

Network switching in the data center



- Open standards
- Interoperable components
- Scalable to any size

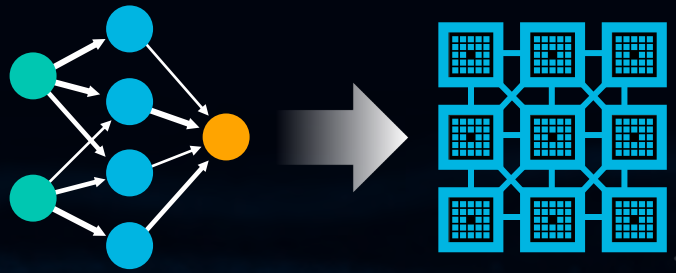
AI calls for enhanced cloud switch architecture

General purpose

One workload,
one processor

Accelerated

One workload,
many connected processors

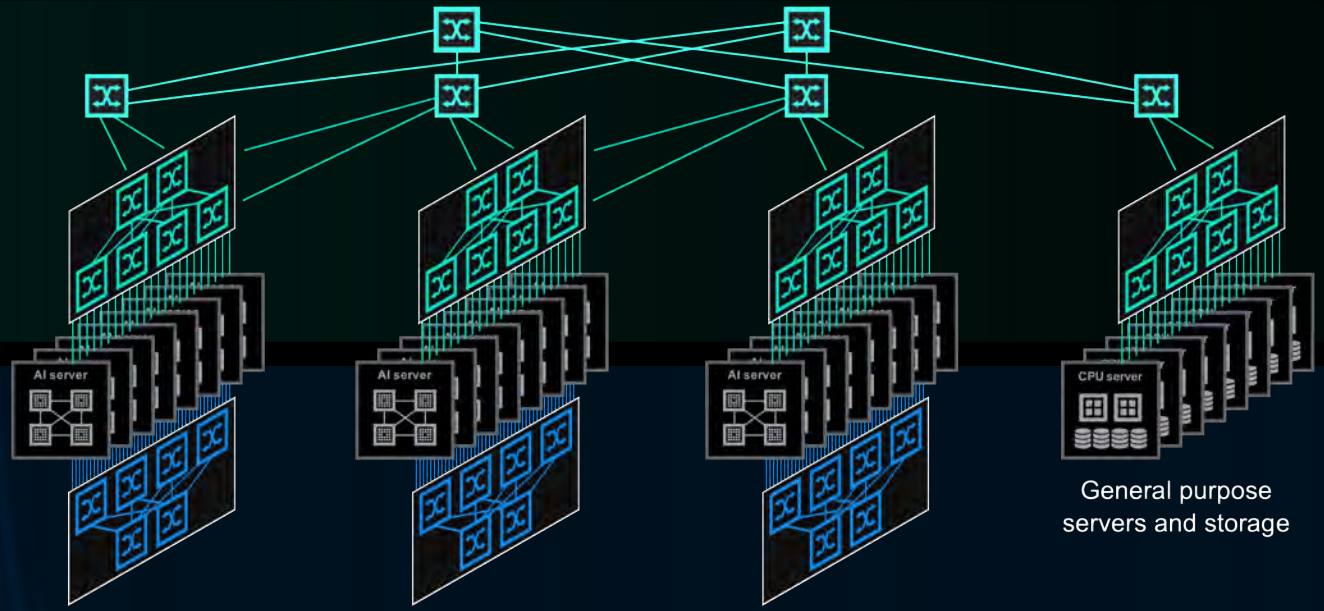


Network performance integral to compute efficiency

Ethernet switching in the AI cloud

Frontend network
Ethernet

Backend network
InfiniBand
Ethernet



Accelerated compute drives significantly more network ports

Switching is a semiconductor **tour de force**

Single-chip **multi-terabit packet switch**

with on-chip

- Packet buffer
- Route tables
- Telemetry

Maximum capacity

Advanced process

High-speed serial I/O

Low latency

Power efficient

Marvell cloud switch: a market breakthrough

Innovium™

12.8 Tbps

- Clean sheet architecture for cloud
- Delivered at leading speed
- Tier 1 hyperscale design win
- Deployed at high scale

Marvell AI cloud network switch

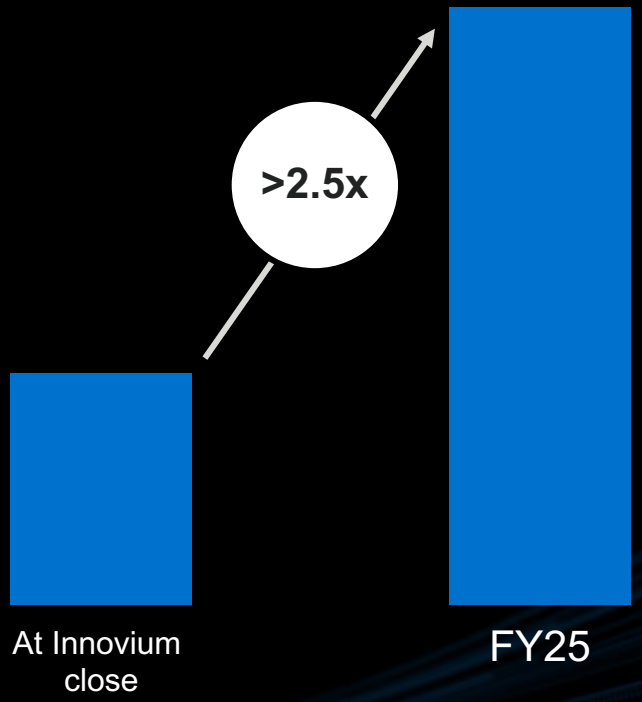
> 60 billion transistors

- 51.2 Tbps with 100G SerDes
- Marvell 5nm implementation
- Programmable and low latency
- Production summer 2024

New OEM customer design wins

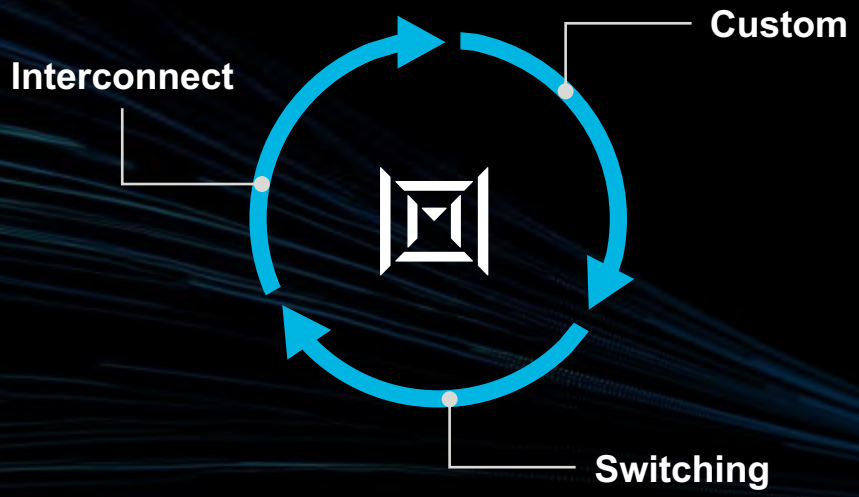
Increased investment in AI cloud switching

Marvell data center switch team



- Consolidated switch organization
- Expanded silicon roadmap
- Increased software and support

Marvell tech portfolio enables switch roadmap

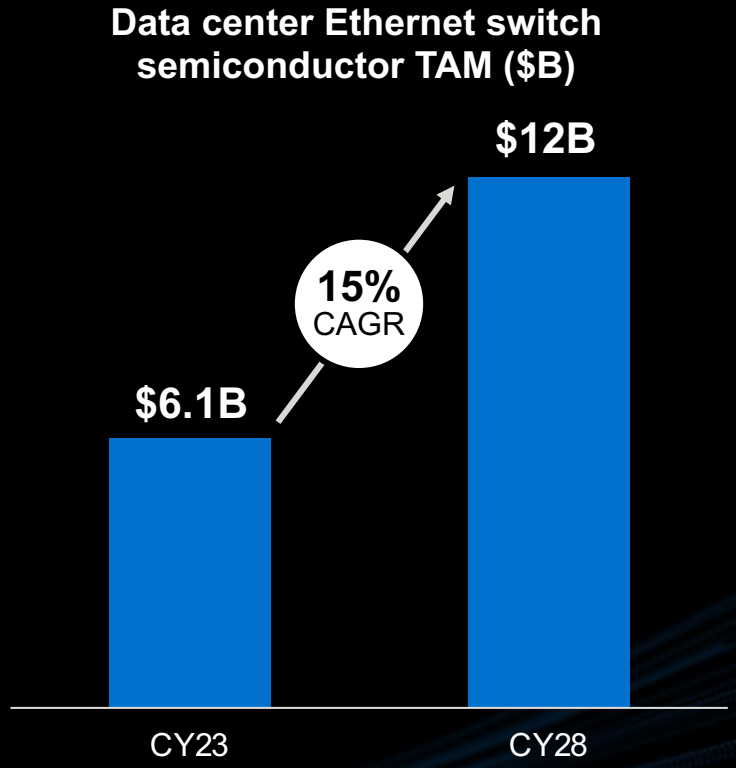


- 3nm and 2nm foundational IP
- 224G SerDes and beyond
- Advanced packaging and assembly
- Silicon photonics

AI motivating cloud switch innovations

	Past	AI era
Open platforms	Proprietary OS software Vendor-specific silicon	Open network OS Hardware abstraction layer
Workload awareness	Load balancing	Congestion management Traffic engineering
Network architecture	Build a bigger switch	Blurred boundaries of switch and interconnect Novel repartitioning of large cloud fabrics

Data center switch market



- $6B TAM across WW data centers
- 15% CAGR
- AI switching growing at faster rate

Source: 650 Group

Marvell switch business accelerating

Multi-billion $ opportunity

New customers

51.2T production summer 2024

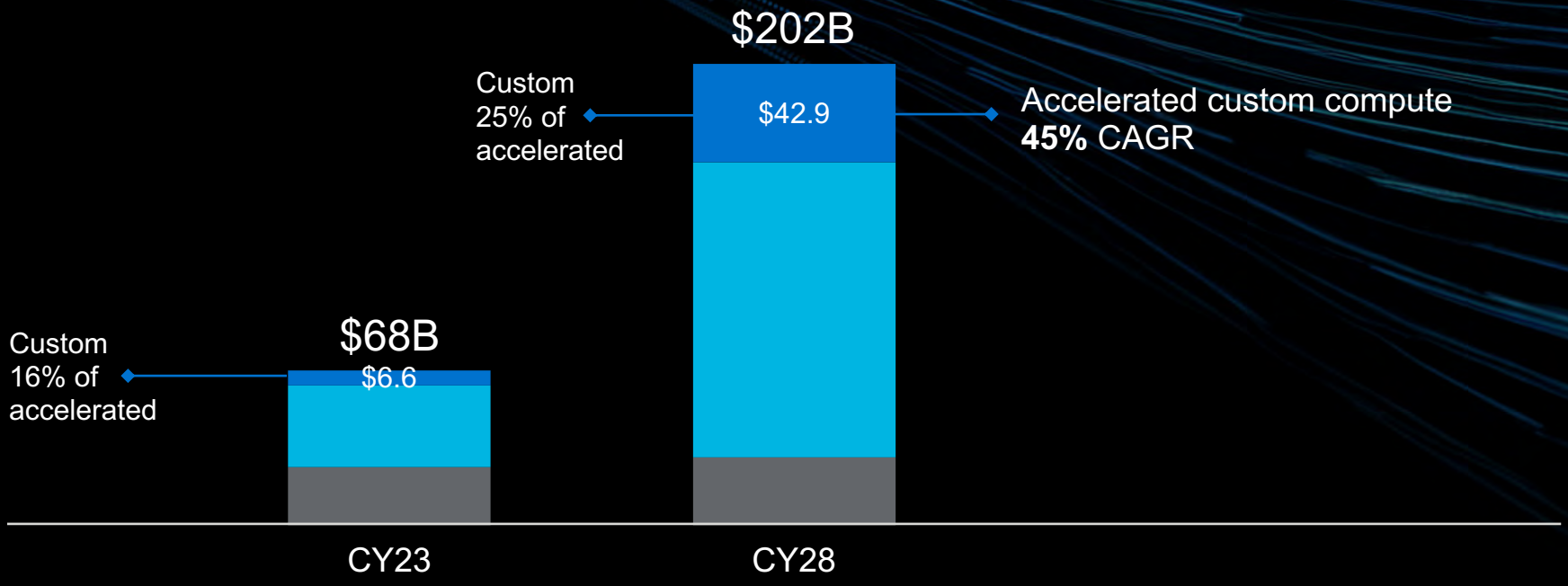
Raghib Hussain

President, Products and Technologies

CAVIUM

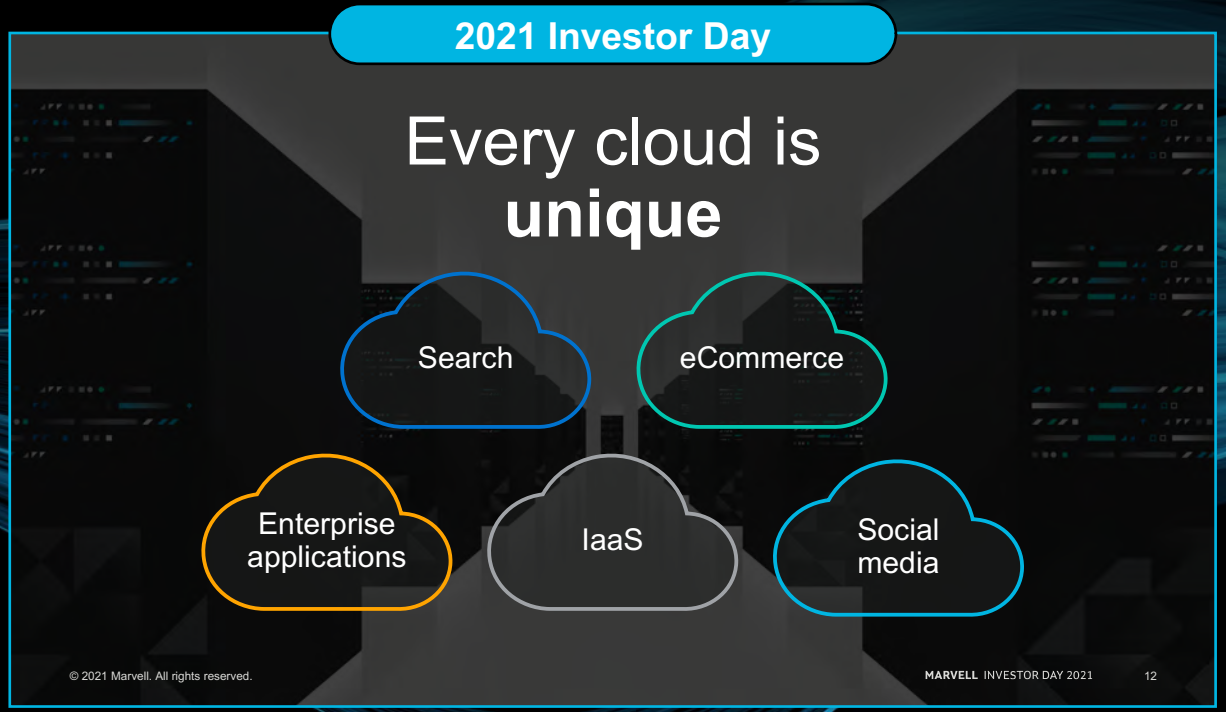
Industry's first accelerated compute for networking

Data center **custom compute** opportunity



Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates

Why custom compute?



Multiple business models within cloud

Internal applications	Software as-a-service (SaaS)	Infrastructure as-a-service (IaaS)
▪ Google search ▪ Bing search ▪ Amazon.com ▪ Instagram	▪ Microsoft Copilot ▪ Amazon Bedrock ▪ Google Vertex AI ▪ OCI Gen AI ▪ Snowflake Cortex AI ▪ OpenAI ▪ Databricks Mosaic AI	▪ Azure AI ▪ Google AI ▪ AWS EC2 ML ▪ Oracle AI

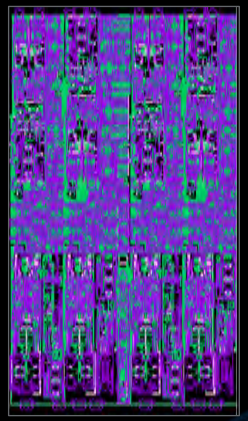
Custom silicon adoption

Marvell accelerated infrastructure platform

Process node

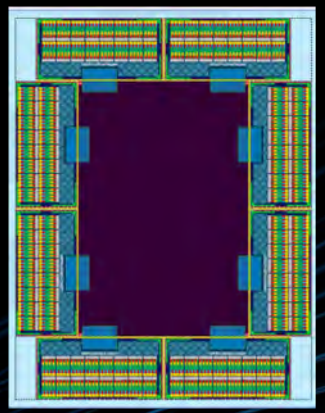
- 5nm
- 3nm
- 2nm

IP



SerDes

Packaging

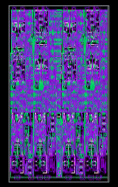
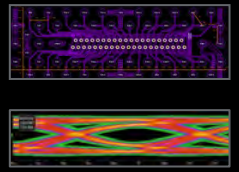
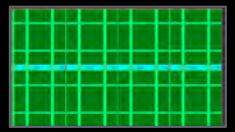
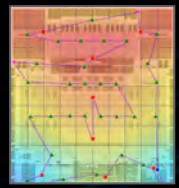
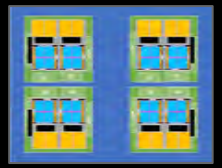
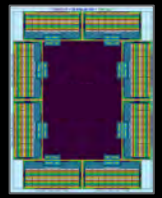
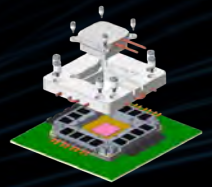


2.5D/3D

Expertise

- Processor
- Large silicon
- Multi-chip
- Chiplet
- High bandwidth
- Networking
- SiPho

Significant R&D scale and IP leadership required

High-performance SerDes	Chip-to-chip (D2D) interconnect	Ultra-high density & low power SRAM	HBM chiplet	In-house tools
				
Advanced substrates	**2.5D / 3D packaging**	**CoWos-S CoWos-R**	**Advanced thermal solutions**	**3D SiPho integration**
				

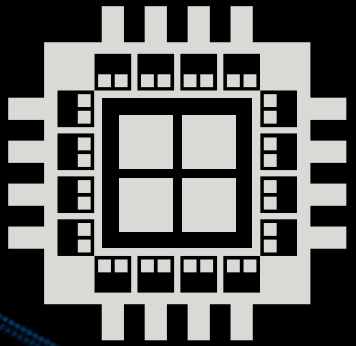
Pushing the boundary of technologies

Expertise and experience

1990
1M transistors

- Functional
- Timing

Now
>100B transistors



- Functional and timing
- Cross-die timing
- Multi-chip
  - Power
  - Connectivity
  - Thermal
- Signal integrity
- Mechanical stress

Only large infrastructure companies can succeed

Decades of world-class IP

Significant investment in complete custom platform

Multiple custom compute opportunities

Accelerated compute for AI

XPU

CPU

Custom compute

Security

NIC / DPU

Arm compute

Storage

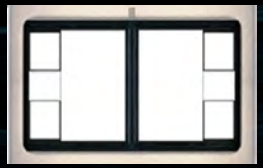
Video

CXL

Multiple custom compute products

Accelerated compute for AI

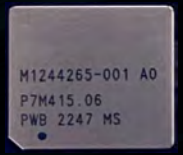
XPU



CPU

Custom compute

Security



NIC / DPU

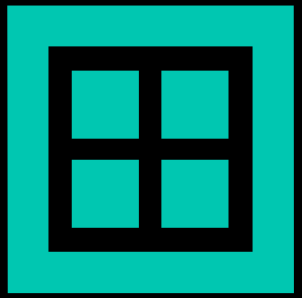
Arm compute

Storage

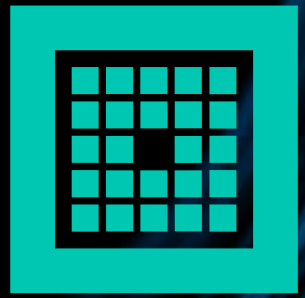
Video

CXL

Two custom compute examples

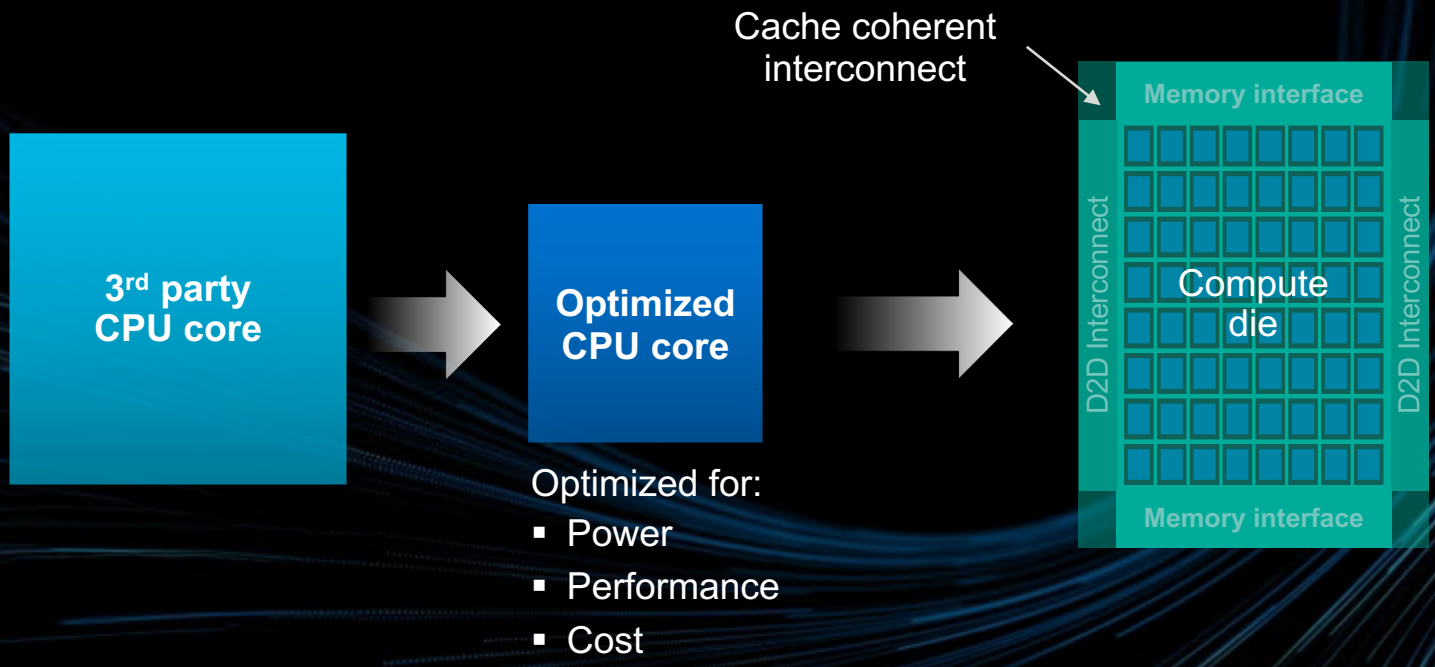


CPU



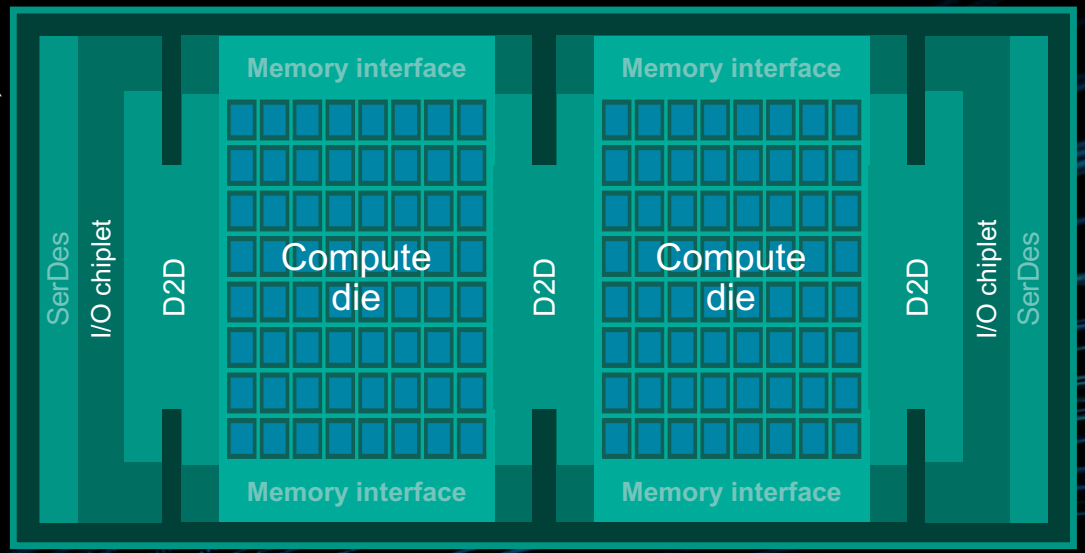
AI accelerator

Putting it all together: CPU custom compute



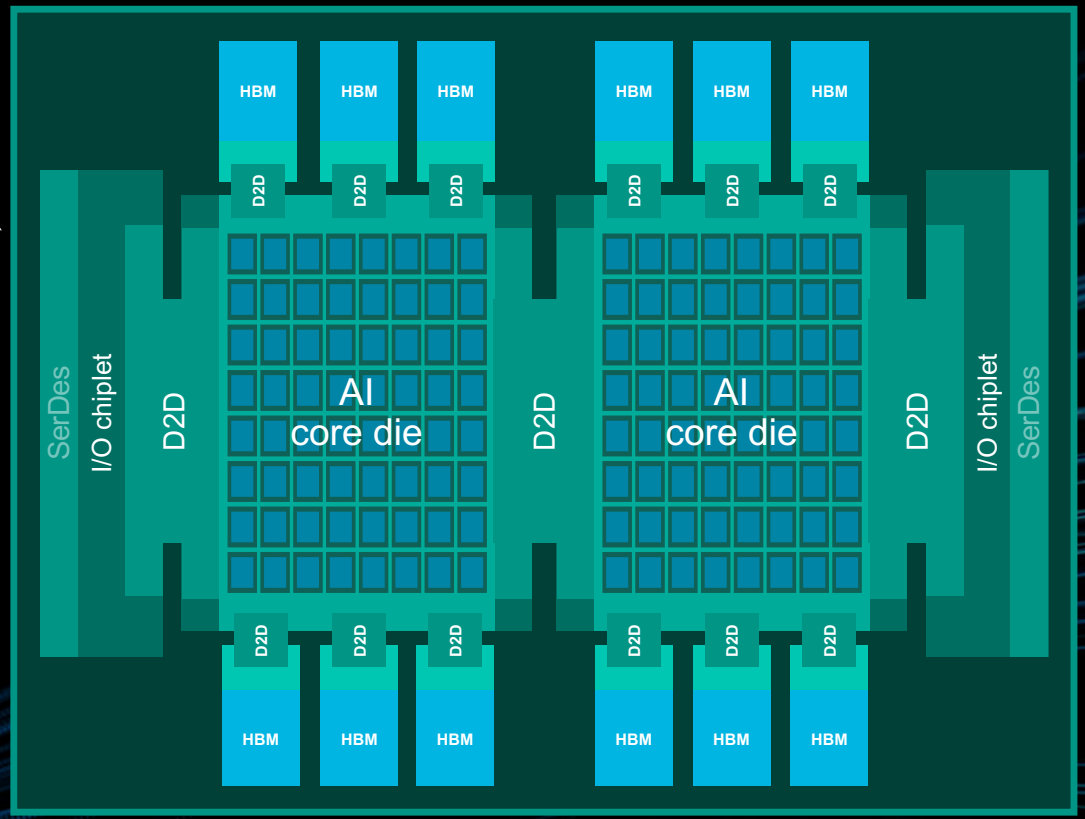
Custom compute CPU

Decades of experience in building complex compute SoCs



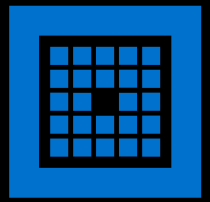
Custom AI Accelerator

Decades of experience in building complex compute SoCs



Expanding our AI customer base

Customer A



AI training accelerator

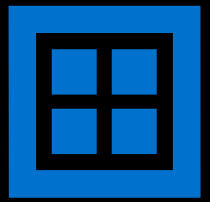
Ramping now

AI inference accelerator

CY2025 ramp

NEW!

Customer B



Arm CPU

Ramping now

NEW!

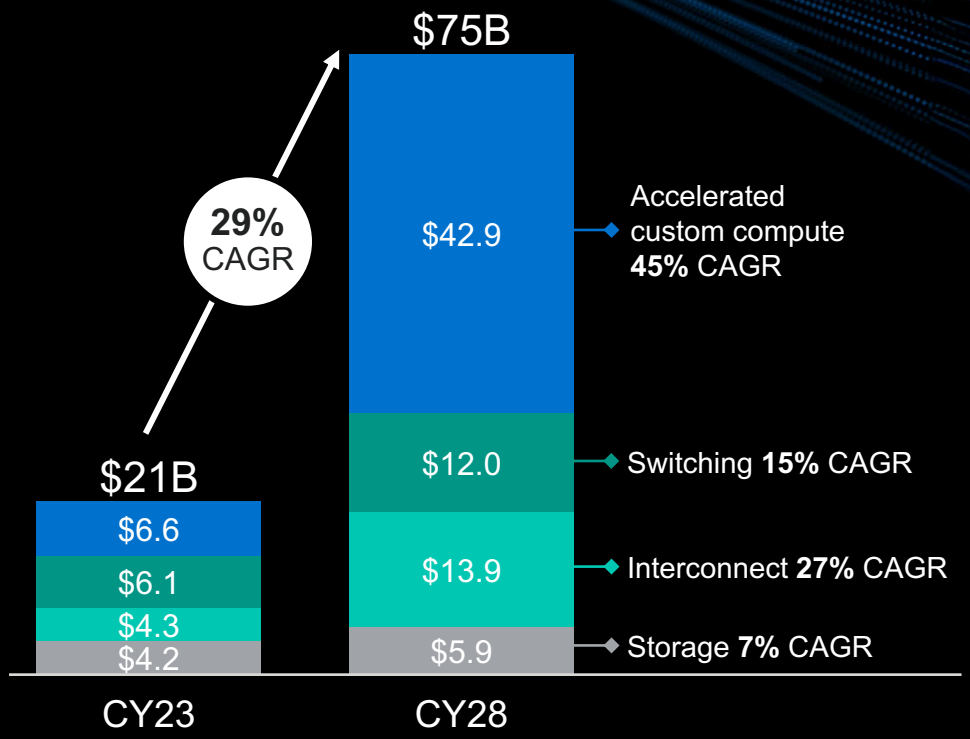
Customer C

AI accelerator

CY2026 ramp

AI compute: 3 out of 4 U.S. hyperscale operators

Fast growing market, expanding share



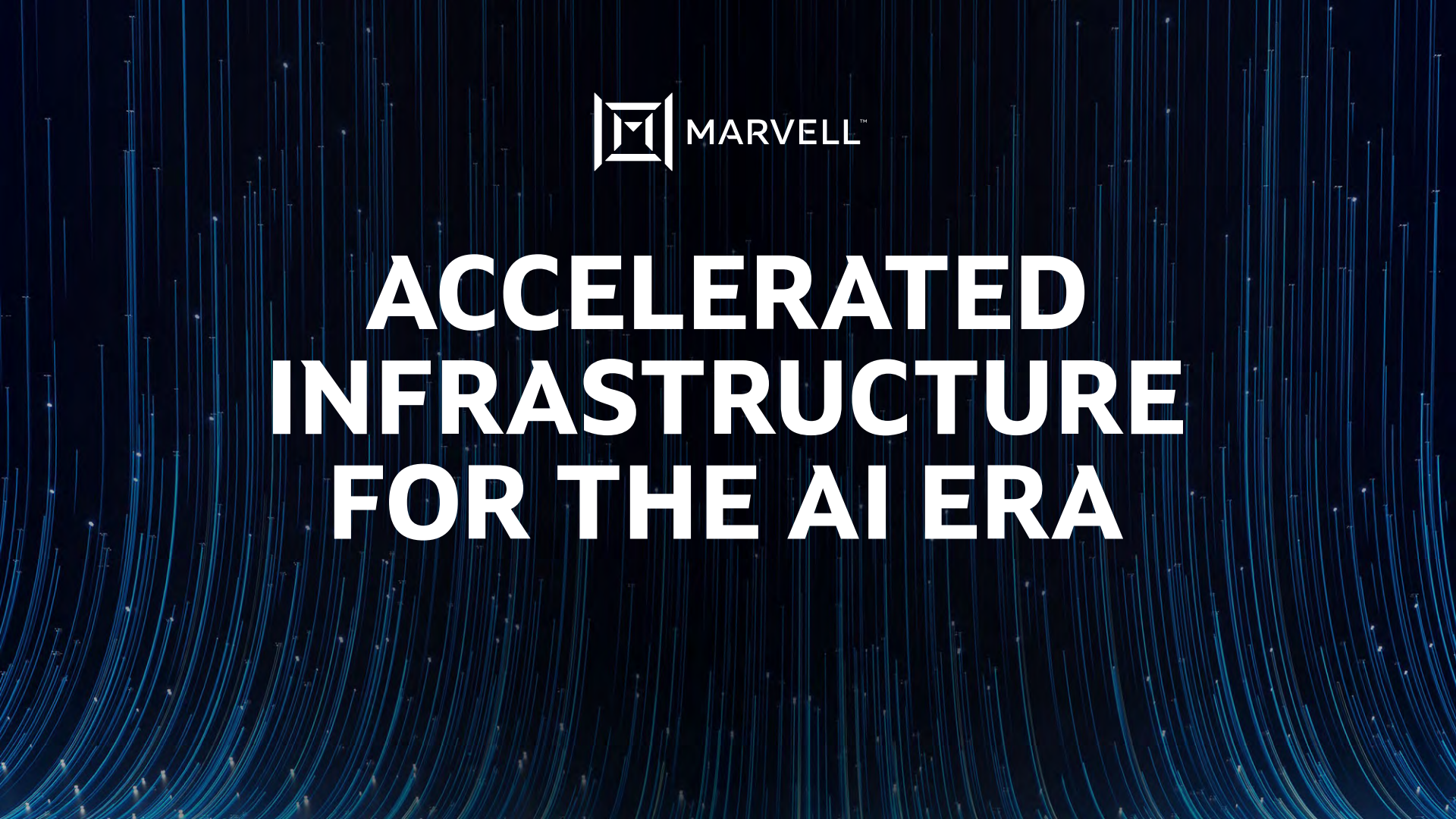
Last year: ~10% share

End-market	Share expectations
Accelerated custom compute	Gain
Switching	Gain
Interconnect	Maintain
Storage	Maintain

Long-term target: 20% share

Source: 650 Group, CignalAI, Dell'Oro, LightCounting, and Marvell estimates


MARVELL
Thank you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